SCM1702A CC/CV Primary-Side Regulator

Features

- Primary-side regulation eliminates optocoupler
- Built-in loop compensation
- Built-in 650V start-up switch
- Built-in 650V power MOSFET
- Output rectifier forward drop temperature variations compensation
- Wide VDD range allows small bias capacitor
- Large capacitive loading with self-power at start-up state
- Over-voltage, over-temperature and over-current protection
- FB pin and CS pin fault protection

Applications

- USB-compliant adapters and chargers for consumer electronics.
- Auxiliary power supplies

Functional Description

SCM1702A is a flyback primary side power supply controller. It provides isolated Constant Voltage (CV) and Constant Current (CC) output without using an opto-coupler. The device processes information from the primary power switch and an auxiliary flyback winding for precise control of the output voltage and current. With its internal 650V startup switch, the SCM1702A can be started in a wide range of input voltage, and being supplied by the transformer auxiliary winding, the chip’s power consumption remains relatively low.

The SCM1702A controller provides high performance, output precision, advanced dynamic response and low output temperature coefficient due to numerous built-in auxiliary and compensation functions. The built-in functions include protection for over temperature, output overvoltage and over current, feedback (FB pin) and current share (CS pin) faults, so the safety requirements can be easily met.

Typical Application Circuit

![Typical Application Circuit Diagram]

Functional Curve

[Graph showing Output Voltage and Efficiency vs Output Current]

Product package: SOP-7.
Please see “Ordering Information” for details.
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Pin Description

<table>
<thead>
<tr>
<th>NUMBER</th>
<th>NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>I</td>
<td>The VDD input pin is the bias-supply from the transformer auxiliary winding to the controller. It requires a bypass capacitor to GND (VSS).</td>
</tr>
<tr>
<td>2</td>
<td>FB</td>
<td>I</td>
<td>This pin is connected to a voltage divider between an auxiliary winding and GND. The ratio of the upper resistor to the lower resistor is used to set the output voltage. The value of the upper resistor of this divider is also used to program the line compensation at the CS pin.</td>
</tr>
<tr>
<td>3</td>
<td>CBC</td>
<td>I</td>
<td>The cable compensation pin can be used for programming the compensation of cable voltage drop.</td>
</tr>
<tr>
<td>4</td>
<td>CS</td>
<td>I</td>
<td>Current sense PIN</td>
</tr>
<tr>
<td>5</td>
<td>D</td>
<td>O</td>
<td>This connects to the internal MOSFET drain and the high voltage (D) pin may be connect directly to the transformer, providing the charge current to the VDD capacitor for starting up the power supply.</td>
</tr>
<tr>
<td>6</td>
<td>VSS</td>
<td>P</td>
<td>The VSS ground (GND) pin is both, the controller reference pin and the drive outputs low-side return. Special care must be taken to keep all AC-decoupling capacitors returns as close as possible to this pin and avoiding any lengthy common traces with analog signal return paths.</td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), voltage reference is ground.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias Supply Voltage, VDD</td>
<td>VDD</td>
<td>22</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>D Pin Voltage</td>
<td>VDS</td>
<td>-0.6</td>
<td>650</td>
<td>V</td>
</tr>
<tr>
<td>Control pin voltage (FB, CS, CBC)</td>
<td>VFB, VCS, VCBC</td>
<td>-0.6</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>Tj</td>
<td>-40</td>
<td>150</td>
<td>℃</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>TSTG</td>
<td>-40</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>Lead Temperature 0.6 mm from Case</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electro Static Discharge (ESD) rating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Human Body Model (HBM)</td>
<td></td>
<td>2000</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Charged Device Model (CDM)</td>
<td></td>
<td>1000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rms Current Of Power MOSFET</td>
<td>I_DDP, I_DSP</td>
<td></td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>Maximum Dissipation Power</td>
<td>P_TOT</td>
<td></td>
<td></td>
<td>mW</td>
</tr>
</tbody>
</table>

Important: Exposure to absolute-maximum-rated conditions for extended periods may severely affect device reliability, stress levels exceeding the “Absolute Maximum Ratings” may result in permanent damage.

### Recommended Operating Conditions

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), V_DD=12V, GATE=no load.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias supply operating voltage</td>
<td>VDD</td>
<td>9</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>VDD bypass capacitor</td>
<td>CVDD</td>
<td>0.047</td>
<td>20</td>
<td>uF</td>
</tr>
<tr>
<td>Full Load Operating frequency</td>
<td>F_SW</td>
<td>68</td>
<td>120</td>
<td>kHz</td>
</tr>
<tr>
<td>Operating junction temperature</td>
<td>Tj</td>
<td>-40</td>
<td>125</td>
<td>℃</td>
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</table>

### Electrical Characteristics

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), V_DD=12V, GATE=no load.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>HIGH VOLTAGE STARTUP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_STL</td>
<td>Startup Current out of VDD</td>
<td>V_D=100V, V_DG=0V. Startup current out of VDD</td>
<td>250</td>
<td>400</td>
<td>550</td>
<td>uA</td>
</tr>
<tr>
<td>I_STH</td>
<td>Startup Current out of VDD</td>
<td>V_D=100V, V_DG=5V. Startup current out of VDD</td>
<td>0.8</td>
<td>2.5</td>
<td>4</td>
<td>mA</td>
</tr>
<tr>
<td>I_STL_KG</td>
<td>Leakage Current at V_N</td>
<td>V_VN=400V, run state</td>
<td>1</td>
<td></td>
<td></td>
<td>uA</td>
</tr>
<tr>
<td>I_VDD_STATE</td>
<td>Static Supply Current</td>
<td>I_GATE=0</td>
<td>400</td>
<td>550</td>
<td>700</td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td><strong>UNDERRVOLTAGE LOCKOUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_VDD_ON</td>
<td>VDD Turn-on Threshold</td>
<td>V_VDD low to high</td>
<td>15</td>
<td>16.25</td>
<td>17.5</td>
<td>V</td>
</tr>
<tr>
<td>V_VDD_OFF</td>
<td>VDD Turn-off Threshold</td>
<td>V_VDD high to low</td>
<td>7.8</td>
<td>8.4</td>
<td>9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td><strong>CS INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RLC</td>
<td>Internal Line Compensation Resistance</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>V_CST_MAX</td>
<td>Max CS Threshold Voltage</td>
<td></td>
<td>0.77</td>
<td>0.8</td>
<td>0.83</td>
<td>V</td>
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<tr>
<td>V_CST_MIN</td>
<td>Min CS Threshold Voltage</td>
<td></td>
<td>0.26</td>
<td>0.27</td>
<td>0.28</td>
<td>V</td>
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<tr>
<td>K_AM</td>
<td>PWM Control Ratio</td>
<td></td>
<td>3</td>
<td></td>
<td></td>
<td>V/V</td>
</tr>
<tr>
<td>K_CL</td>
<td>Line Compensation Current Ratio</td>
<td></td>
<td>23/2</td>
<td></td>
<td></td>
<td>A/A</td>
</tr>
<tr>
<td>K_OS</td>
<td>Maximum Ratio of T_DDP/T</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>S/S</td>
</tr>
<tr>
<td></td>
<td><strong>FB INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_FBIR</td>
<td>Regulating Level</td>
<td>Measured at no-load condition</td>
<td>3.77</td>
<td>3.808</td>
<td>3.846</td>
<td>V</td>
</tr>
<tr>
<td>V_FBNC</td>
<td>Negative Clamp Level</td>
<td></td>
<td>-35</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td><strong>CABLE COMPENSATION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_CFB_MAX</td>
<td>Maximum Cable Compensation Voltage</td>
<td></td>
<td>277</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>V_CFB_MIN</td>
<td>Minimum Cable Compensation Voltage</td>
<td></td>
<td>37.8</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Timing</td>
<td>T_FB_LEB</td>
<td></td>
<td>1.4</td>
<td></td>
<td></td>
<td>uS</td>
</tr>
</tbody>
</table>
**Startup Frequency**

- F_{SW,min} = Minimum Switching Frequency
  - V_{FB}=V_{FBR}
  - 558 Hz
- F_{ON_MAX} = Maximum Gate On-Time
  - CS connect to GND
  - 10.2 kHz
- F_{PD} = Protection Delay Time
  - FB, CS fault or over-temperature state or V_{FBS}=V_{OVP}
  - 6 μs
- F_{VDD,STOP_MAX} = Maximum Startup Switch Supply Time
  - 3072 μs

**PROTECTION**

- V_{GD} = Over voltage Threshold
  - At FB input, T_J = 25 °C
  - 4.12 4.32 4.52 V
- V_{CS} = Over current Threshold
  - At CS input
  - 1.52 1.60 1.68 V
- T_{J,STOP} = Thermal Shutdown Temperature
  - Internal junction temperature
  - 155 °C
- T_{J,RESTART} = Thermal Restart Temperature
  - Internal junction temperature
  - 98 °C

**DRIVERS**

- I_{GTS} = Internal GATE source current
  - V_{VDD}=15V, C_{GS}=1nF
  - 50.2 mA
- V_{GT,CLAMP} = Internal GATE clamp voltage
  - 16.2 17.4 18.6 V
- R_{DS,ON} = Power MOS ON-State Resistance
  - V_{GS}=10V, I_{D}=0.5A
  - - - 16 Ω
- V_{BR,DIS} = Power MOS Breakdown Voltage
  - V_{GS}=0V, I_{D}=250μA
  - 650 - - V
- I_{DS} = OFF-State Current
  - V_{GS}=650V, V_{GS}=0V
  - - - 1 μA

**Typical Curve**

- **Fig. 1**: Bias Supply Current vs. Bias Supply Voltage
- **Fig. 2**: Start-up Current vs. Temperature
**Fig. 3** FB Regulation Voltage vs. Temperature

**Fig. 4** FB Over-voltage threshold vs. Temperature

**Fig. 5** Minimum CS Threshold vs. Temperature

**Fig. 6** Maximum CS Threshold vs. Temperature

**Fig. 7** Minimum Switching Frequency vs. Temperature

**Fig. 8** GATE Source Current vs. Temperature
**Parameter Test Information**

**Fig. 9 Efficiency vs. Load Current**

**Fig. 10 Functional Curve Test Circuit**

**Fig. 11 Definition Of Rise Time and Fall Time**

**Fig. 12 Switching Character Test Circuit**

**Fig. 13 Magnetization Phase Of Flyback Converter**

**Fig. 14 Demagnetization Phase Of Flyback Converter**

**Transformer Work Mode**

**Detailed Application Description**

SCM1702A is an integrated 1A/650V Power MOSFET, with typical application is PSR flyback converter, as shown in Fig. 15. By sensing the auxiliary coil’s voltage, you can sense the output voltage of converter, and realize loop control. You can set the ratio of the resistor Rs1 and Rs2 or the ratio of the turns NS and NA, to set the converter’s output voltage. The feedback voltage feed to the pin FB. By the way, you can also set the cable compensation voltage using a suitable resistor. And with a suitable sensing resistor to the pin CS, you can set the power level of the converter, ie limited current.
**High Voltage Startup Operation**

An internal high voltage startup switch is connected to the primary side of the transformer and continuously charges the VDD capacitor from the voltage of the bulk capacitor C_B, see also Fig. 16.

![Typical Application Circuit](image)

When the VDD voltage is below 2.4V, the built-in startup circuit charges the VDD capacitor with lower current $I_{STL}$. When the VDD voltage exceeds 2.4V, the built-in startup circuit charges the VDD capacitor with higher current $I_{STH}$. When VDD reaches $V_{DD\_ON}$ the controller is enabled, the converter starts switching, the high voltage startup switch continues charging the VDD capacitor until the VDD voltage is 20.8V. The VDD voltage starts to drop once the controllers run state current becomes larger than the high limit of the startup current. The controller is self-power and independent from VDD voltage changes. The maximum self-powered on time of the supply is $T_{VDD\_STOP\_MAX}$ and self-power stops either when the converter output voltage reaches the target voltage $V_{OUT\_CV}$ or the converter into protected state. Refer to Electrical Characteristics for $I_{STL}$, $I_{STH}$, $V_{DD\_ON}$ and $T_{VDD\_STOP\_MAX}$ values.

**Over Current point (constant current point) Design**
The SCM1702A controller sets the ratio (KGS) between the demagnetization time TDEM and the switching period TSW. The secondary average output current IO_MAX is determined by the primary peak current, the turns-ratio, the demagnetization time TDEM and the switching period TSW:

\[ I_{O\_MAX} = \frac{1}{2} \cdot \frac{N_p}{N_S} \cdot K_{DS} \cdot \eta_{XFMR} \cdot I_{PEAK\_MAX} \quad (1) \]

where

\( N_p/N_S \) is the transformer primary to secondary turns-ratio (a typical ratio for 5V output is 13 to 15)

KGS is the ratio of the demagnetization time and the switching period TDEM/TSW

\( \eta_{XFMR} \) is the transformer efficiency at full power

\( I_{PEAK\_MAX} \) is the maximum of primary peak current.

The over current point design of the transformer is modulated through \( N_p/N_S \) and \( I_{PEAK\_MAX} \). In CC mode, the controller defined the KGS ratio (ratio of demagnetization time TDEM and switching period TSW). The over current point is confirmed, once the parameters of the transformer and the maximum primary peak current are established.

\[ I_{PEAK\_MAX} = \frac{V_{\text{CST\_MAX}}}{R_{CS}} \quad (2) \]

**Example:** With a transformer core and winding loss of 5%, a primary to secondary leakage inductance of 3.5% and bias power to output power ratio of 0.15%, the \( \eta_{XFMR} \) value at full power is approximately: \( \eta_{XFMR} = 1.05-0.035-0.015 = 0.9 \).

A converter design of 5V/0.6A (3W) has an over current capacity of 10% and a transformer primary to secondary turns ratio of 14. The current sense resistor value is calculated as follows:

\[ R_{CS} = \frac{V_{\text{CST\_MAX}}}{2 \cdot I_{O\_MAX}} \cdot \frac{N_p}{N_S} \cdot K_{DS} \cdot \eta_{XFMR} \quad (3) \]

\[ = \frac{0.8}{2 \times 0.66} \times 14 \times 0.5 \times 0.9 \]

\[ = 3.8 \Omega \]

**Output Voltage Design**

The waveform of the auxiliary winding consists of three parts as shown in Fig. 17. The first part is the MOSFET switch on time T_ON, where the voltage is \( V_{\text{BULK}}/N_A \). The second part is demagnetization time TDEM, the voltage is \( (V_{\text{OUT}}+V_F) \) NA0. The third part is primary inductance and capacitance resonance time \( T_{RING} \).

![Fig. 17: Auxiliary winding, detailed waveform](image)

The SCM1702A includes an FB signal sampler, employing signal discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are however some details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. A detailed illustration of waveform and criteria to ensure a reliable sample on the FB pin is shown in Fig. 17. The first detail to observe is the duration of the leakage inductance reset pedestal \( T_{LK\_RESET} \), because this can mimic the waveform of the secondary current decay, followed by a sharp downslope. It is important to keep the leakage reset time smaller than the FB sample blank time \( T_{BLK\_LB} \). The second detail observed is the amplitude of ringing on the \( V_{\text{BULK}} \) waveform following \( T_{LK\_RESET} \). The peak to peak voltage at the FB pin should be less than approximately 100m/Vp-p at least 200 ns before the end of the demagnetization time. In constant voltage mode, the output voltage has the following relation:

\[ V_{\text{OUT\_CV}} = \frac{N_S}{N_A} \cdot (1 + \frac{R_{S1}}{R_{S2}}) \cdot V_{FBR} - V_F \quad (4) \]

Where

\( N_p/N_S \) is the transformer primary to secondary turns-ratio

\( R_{S1} \) is the high-side resistor value of the VS divider

\( R_{S2} \) is the low-side resistor value of the VS divider

\( V_{\text{FBR}} \) is the CV regulation level at the VS input (see the table),

\( V_F \) is the output rectifier forward drop at near zero current.
During CV regulation, the frequency and amplitude modulation modes are shown in Fig. 18, where $I_{FP}$ and $F_{SW}$ is normalized curves relative to the output of the error amplifier. The FB feedback signal is filtered by a compensation filter and results in the output of the error amplifier. The value of the output of EA is approximately equal to FB voltage at steady state. The controller limits the maximum switching frequency $F_{SW,\text{MAX}}$ and the minimum switching frequency $F_{SW,\text{MIN}}$ (see electrical characteristics). The recommended operating switching frequency is between 68kHz and 110kHz and higher switching frequencies affect the converters efficiency and EMI performance. The maximum switching frequency is defined by the primary inductor and the primary peak current (see also switching frequency design).

The FB sampling time $T_{FBLEB}$ is fix at 1.4us. The minimum demagnetization time $T_{DEM}$ is the smallest under light load peak current. Therefore the design must ensure that under light load condition, $T_{DEM}$ minimum is greater than the FB sampling time $T_{FBLEB}$. As shown in the formula (5), it is recommended to set $T_{DEM,\text{MIN}}\geq 2 \cdot T_{FBLEB}$.

\[ T_{DEM,\text{MIN}} = \frac{L_m \cdot V_{CST,\text{MIN}}}{R_{CS} \cdot \frac{N_p}{N_s} \cdot V_{OUT}} \geq 2 \cdot T_{FBLEB} \quad (5) \]

\[ V_{CFB} = \left( \frac{V_{EA} - V_{GSN}}{66.1k\Omega + (14.9k\Omega + R_{CBC}) \cdot 264.3k\Omega} - 4\mu A \right) \times \frac{2}{5} \times 24.4k\Omega \quad (6) \]

\[ V_{EA} = 4.6V \text{ at maximum load, and } V_{EA} = 1.5V \text{ at minimum load} \]

$V_{GSN}$ is the N-MOSFET gate to source voltage. $V_{GSN} = 2V$ at maximum load and $V_{GSN} = 1.1V$ at minimum load

$R_{CBC}$ is a resistor between CBC pin and ground

When the CBC pin is open ($R_{CBC} = 0$), $V_{CFB,\text{MIN}} = 37.8mV$ at maximum load and the sample voltage on the FB pin is stable at $V_{FB} + V_{CFB,\text{MIN}}$. When the CBC pin is connected to ground ($R_{CBC} = 0$), $V_{CFB,\text{MAX}} = 277mV$ at minimum load and the sample voltage on the FB pin is stable at $V_{FB} + V_{CFB,\text{MAX}}$.

### Temperature Compensation

In offline flyback converters, the secondary side rectifiers used are generally diodes and their forward voltage drop has a negative temperature coefficient which will reduce the output voltage accuracy in PSR.

SCM1702A has an integrated temperature compensation. By detecting the forward voltage of a PN junction in the chip, a voltage $V_{BE}$ results. Then the voltage $V_{BE}$ is reduced to 1/3 and results in compensation voltage $V_{TC}$. This $V_{TC}$ voltage is being overlaid over the FB pin regulation voltage level. $V_{TC}$ also includes negative temperature coefficient, thus compensating for the diode forward voltage drop.

The specified value of $V_{FB}$ in electrical characteristics, is compensated for temperature internally. Therefore $V_{FB}$ in equation (5) can be used to directly calculate the output voltage.

### Switching Frequency

![Fig. 18: Frequency and Amplitude Modulation Modes](image-url)
Once the constant current and over current points are established, then both the maximum primary peak current $I_{PEAK\_MAX}$ as well as the over power point $P_{O\_MAX}$ are confirmed. The maximum switching frequency of the converter is calculated as follows:

$$F_{SW\_MAX} = \frac{2 \cdot P_{O\_MAX}}{L_M \cdot I_{PEAK\_MAX}^2 \cdot \eta_{XFMR}} \quad (7)$$

Modulate $L_M$ to acquire $F_{SW\_MAX}$. SCM1702A’s maximum frequency limited to 168kHz.

### Line Sensor Compensation

The waveform of the auxiliary winding consists of three parts as shown in Fig. 10: First part is the MOSFET switch on time $T_{ON}$, where the voltage is $V_{BULK}/N_{PAK}$. Second part is demagnetization time $T_{DEM}$, the voltage is $(V_O+V_F)N_{BAK}$. Third part is primary inductance and capacitance resonance time $T_{RING}$. According to the flyback converter concept, the voltage is $V_{BULK}/N_{BAK}$ when the MOSFET switch is on and $T_{ON}$ time and $T_{DEM}$ time are two separate parts. The line sensor uses the FB pin voltage during $T_{ON}$ time. This patented method (patent pending), simply works by clamping the FB voltage with a NPN bipolar transistor during the MOSFET on-time. This pin also senses the FB current generated through $R_S$, by the reflected bulk capacitor voltage to provide run and stop thresholds for AC-input and to compensate the current sense threshold across the AC input range. The line sensor current is given by:

$$I_{COMP} = \frac{1}{K_{LC}} \cdot \frac{N_A}{N_p} \cdot V_{IN} - V_{FBNC} \quad (8)$$

The line sensor voltage $V_{RCL}$ realizes the feed forward compensation and ensures the consistency of the over current point at the high and low voltage level. The voltage of the feed forward resistance $R_{LC}$ can be calculated by the following formula:

$$V_{RCL} = I_{COMP} \times R_{LC} = \frac{V_{IN} \times T_D}{L_P} \times R_{CS} \quad (9)$$

$T_D$ is the total current sense delay consisting of the MOSFET turnoff delay, plus an internal delay of approximately 50ns

$L_P$ is the transformer primary inductance

$V_{FBNC}$ is the negative clamp level of the FB pin (see electrical characteristics)

$K_{LC}$ is line compensation current ratio (see electrical characteristics)

$R_{CS}$ is the value of the SCM1702A controllers internal line sensor resistor (see electrical characteristics)

### Fault Protection

SCM1702A controller provides extensive fault protection including the following:

- Output short to ground protection
- Output over voltage protection
- FB pin fault protection
- CS pin fault protection
- Internal over temperature protection

**NOTE:** The following Fig.s 18 and 19 show the controller just after start-up. VDD is the voltage at the VDD pin, $C_{VDD}$ is the VDD bypass capacitor and $V_{GATE}$ is the pulsating voltage of the gate driver.

### Output Short protection

During the first stage shown in Fig. 19, the controller can’t get power from auxiliary winding if the output is shorted, then the VDD bypass capacitor voltage starts to drop, the controller can't output any gate pulse until the VDD bypass capacitor voltage drops to $V_{VDD\_OFF}$ level (see electrical characteristics).
In the second stage, the controller stops to generate gate pulses when \( V_{\text{DD}} = V_{\text{DD, OFF}} \), the internal high voltage startup device is active until \( V_{\text{VDD}}^T = V_{\text{DD, ON}} \). The typical startup current \( I_{\text{TH}} \) (see electrical characteristics) provides fast charging of the VDD capacitor. The controller’s power consumption causes \( V_{\text{DD}} \) to fall below \( V_{\text{DD, OFF}} \) again and the GATE can’t output a driver signal during this time. The second stage time is longer than the first stage because the power consumption is smaller.

In the third stage, the device returns to the start state and a startup sequence is initiated. The internal high voltage startup device is active until \( V_{\text{VDD}}^T = V_{\text{DD, ON}} \).

If the output to ground short remains, the above process, also called UVLO process, repeats itself periodically until the short circuit is removed.

The over current point is limited by the chip, meaning that if the converter is over loaded, then the output voltage will drop to maintain the output power constant. The controller cannot get any power from the auxiliary winding because the output has dropped to the lower limit and the controller will repeat the same process.

**Output Overvoltage Protection**

The output overvoltage function is determined by the voltage feedback on the FB pin \( V_{\text{FB}} \). If the stage when \( V_{\text{FB}} \geq V_{\text{OVP}} \) exceeds the \( T_{\text{PD}} \) delay time, the device stops switching and the internal current consumption will let the VDD capacitor voltage drop to \( V_{\text{DD, OFF}} \). Consequently, the device returns to the start state and enters a startup sequence as shown in Fig.20.

![Fig. 20: Timing and waveform of output over voltage protection](image)

**Fault Protection, FB Pin**

If the FB is short cut, open circuit or \( R_{\text{FB}} \) is disconnected for the duration of the delay time \( T_{\text{PD}} \), the SCM1702A will stop switching. Then the SCM1702A goes into an UVLO reset/restart sequence.

**Fault Protection, CS Pin**

The SCM1702A always operates with cycle-by-cycle primary peak current control with a normal operating voltage range of the CS pin between 0.8V and 0.27V. Once An the CS pin voltage reaches 1.6V for the duration of the delay time \( T_{\text{PD}} \), an additional protection that is not filtered by leading-edge blanking sets in, which the results in an UVLO reset/restart sequence of the controller.

**Over Temperature Protection**

The device initiates an UVLO reset cycle if the junction temperature reaches the internal over temperature-protection threshold \( T_{\text{J,STOP}} \) as described in Electrical Characteristics. When the temperature remains the threshold at end of the UVLO cycle, the protection cycle repeats itself and only once the temperature falls below \( T_{\text{J,RESTART}} \) (see electrical characteristics), the device exits the protection mode and resumes normal operation.
Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Type</th>
<th>No. of Pins</th>
<th>Silk Screen Marking</th>
<th>Reel Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCM1702ASA</td>
<td>SOP-7</td>
<td>7</td>
<td>SCM1702ASA YM</td>
<td>3K/REEL</td>
</tr>
</tbody>
</table>

Product marking
SCM1702XYZ:
(1) SCM1702 = Product designation.
(2) x = Version information (Letter from A-Z).
(3) y = Package definition; (S = SOP package).
(4) Z = Operating temperature range (C = 0℃ to +70℃, I = -40℃ to +85℃, A = -40℃ to +125℃, M = -55℃ to +125℃).
(5) YM = Date code for product traceability; Y = code for production year; M = code for production month.

Mechanical Package Information

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions in millimeters</th>
<th>Dimensions in inches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>1.350</td>
<td>1.750</td>
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<tr>
<td>A1</td>
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<td>1.550</td>
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<td>0.330</td>
<td>0.510</td>
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<tr>
<td>c</td>
<td>0.170</td>
<td>0.250</td>
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<tr>
<td>D</td>
<td>4.700</td>
<td>5.100</td>
</tr>
<tr>
<td>e</td>
<td>1.270 (BSC)</td>
<td>0.050 (BSC)</td>
</tr>
<tr>
<td>E</td>
<td>5.800</td>
<td>6.200</td>
</tr>
<tr>
<td>E1</td>
<td>3.800</td>
<td>4.000</td>
</tr>
<tr>
<td>L</td>
<td>0.400</td>
<td>0.800</td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
<td>8°</td>
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Basic Disk Dimensions (mm)

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Load Band Width</th>
<th>B</th>
<th>W1</th>
<th>W2Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOP-7</td>
<td>12</td>
<td>180</td>
<td>12.4</td>
<td>18.4</td>
</tr>
</tbody>
</table>

Technical requirement:

1. Color: Blue (Reference color number;
   PANTONE DS 196-1 C; C100 M70 Y0 K0
   PANTONE DS 197-1 C; C100 M70 Y0 K10
   PANTONE DS 205-1 C; C100 M60 Y0 K20
   PANTONE DS 205-2 C; C85 M50 Y0 K20
   PANTONE DS 206-2 C; C85 M50 Y0 K35
   PANTONE DS 219-1 C; C90 M50 Y5 K15 )

2. Dimensions and tolerances according to ANSI/EIA-481-C-2003;
3. Disk surface good finish, no warping deformation;
4. External packing in good condition, no damage or pollution.

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