MORNSUN®

SCM1101A Highly integrated PWM controller

Features

- Soft-Start Function, Externally Programmable
- Extremely Low Start-up current of 1uA typical
- Frequency Reduction at Light Load and Burst Mode Control under no load
- Programmable Maximum Switching Frequency
- Built-in Slope Compensation.
- Cycle-by-Cycle Current Limiting
- RI Pin Short-to-GND Protection
- VDD Over-Voltage Protection (OVP)
- VDD Under-Voltage Lockout (UVLO)
- Built-in OCP time
- Feedback Open-loop Protection/Short-circuit Protection
- Vin Under-Voltage Protection
- Built-in Feed-forward Compensation Circuit

Package

Mechanical package: MSOP-8
(see “Ordering information” for details).

Applications

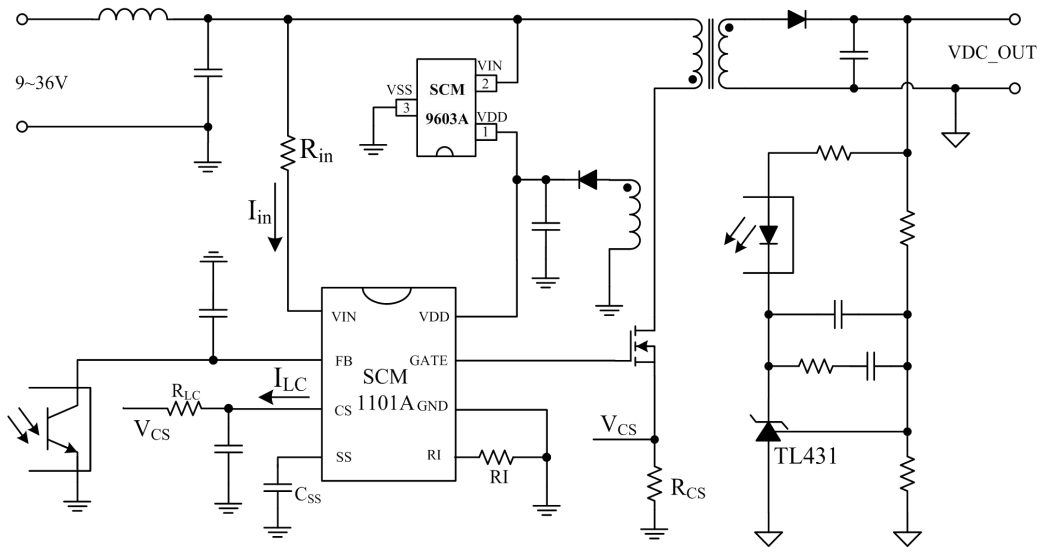
- DC-DC Isolate Converter, recommended power range 5~40W.

Functional Description

This highly integrated SCM1101A current mode PWM controller is ideal for Isolate DC-DC converter applications. The PWM switching frequency is internally adjusted within a tight range. The chip’s maximum working frequency can be changed by means of external resistors. To conserve energy under light load conditions, the green mode function continuously decreases the switching frequency, thus enabling the converter to maintain high efficiency over the entire load range. For optimized standby power consumption, the power supply enters into a burst mode under no load conditions.

The SCM1101A design also integrates a series of protection features that will enhance the power system’s reliability. These functions include Vin Under-Voltage Protection, VDD Under-Voltage Lock Out (UVLO), VDD Over-Voltage Protection, Soft-Start pin SS Suspended Protection, Feedback Open-Loop Protection / Short-Circuit and Overload Protection and CS pin Suspended Protection.

Typical Application Circuit



Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (unless otherwise specified).

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	VDD		23	V
VDD Clamping Current	I_{CLAMP}		10	mA
Gate-drive Voltage (at GATE)	V_{DRV}	-0.6	30	V
Voltage Range	FB,CS,RI	-0.6	6	
	SS	-0.6	6	
Storage Temperature Range	T_{STG}	-55	150	℃
Lead Temperature, Soldering for 10 seconds	Distance 0.6mm from case, 10 sec.		260	
Moisture Sensitivity Level	MSL	MSL3		
Electro Static Discharge (ESD)	Human Body Model（HBM）		3000	V
	Charged Device Module（CDM）		1000	

Important: Stress levels exceeding the “Absolute Maximum Ratings” are not recommended, they may severely affect the device reliability and/or result in permanent damage.

Recommended Operating Conditions

VDD=12V and T_A=25℃, unless otherwise noted

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{VDD}	7.5	14	V
VDD Bypass Capacitor	C_{VDD}	0.047	20	uF
Operating Switching Frequency	F	200	480	kHz
Operating Junction Temperature	T_J	-40	125	℃

Electrical Characteristics

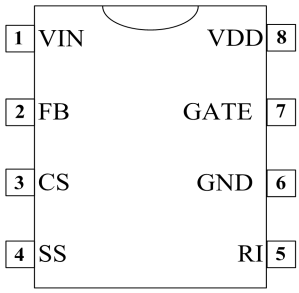
VDD=12V and T_A=25℃, unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Section(VDD Pin)						
I_{START_UP}	VDD Start-up Current	Current flow into VDD port measured at VDD=6V		1	40	uA
I_{VDD_OP}	Operating Supply Current	V_{FB}=3V，RI=24k Ohm	1.0	1.4	2	mA
V_{UVLO_ON}	VDD Turn-on Threshold	VDD Voltage increasing	6.4	7.0	7.6	V
V_{UVLO_OFF}	VDD Turn-off Threshold	VDD Voltage decreasing	5.9	6.4	6.9	V
V_{OVP}	VDD OVP Threshold	VDD from 15V~21V	17	18	19	V
V_{OVP_HYS}	VDD OVP Hysteresis			3.2		V
V_{CLAMP}	VDD Clamping Voltage	the absorption current capacity when VDD increased suddenly	20	22.5	25	V
Feedback Input Section (FB pin)						
A_{V_CS}	PWM Input Gain	$\triangle V_{FB}/\triangle V_{CS}$		3.5		V/V
V_{FB_OPEN}	FB pin Open Voltage			5.3		V
I_{FB_SHORT}	FB pin Short-circuit Current	Current measured when FB pin connected to GND		1.2		mA
Z_{FB_IN}	FB Input Impedance			4.5		kohm
V_{TH_PL}	Power Limiting FB Threshold Voltage			4.5		V
Output Driver Section (GATE pin)						
V_{OL}	Output Low Level	I_O=20 mA(sink)		0.1		V
V_{OH}	output High Level	I_O=20 mA (source)		11.8		V

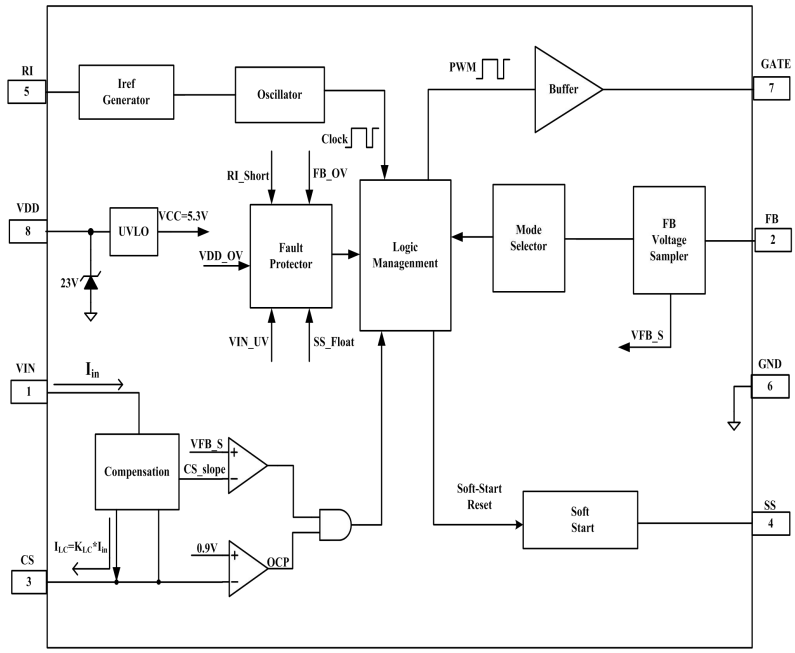
T_R	Output rise Time	C_{GATE}=1nF		20		nSec
T_F	Output Fall Time	C_{GATE}=1nF		20		nSec
Oscillator Section (RI pin)						
F_{OSC}	Oscillator Frequency	RI=24K	285	305	325	kHz
$\triangle F_{TEMP}$	Frequency Temperature Stability	-40℃ ~ 125℃		5		%
$\triangle F_{VDD}$	Frequency Voltage Stability	V_{VDD}=7~16V		5		%
D_{MAX}	Maximum Duty Cycle		74	78	82	%
RI_{RANGE}	RI Operating Range		15	24	48	k ohm
V_{RI_OPEN}	RI Pin Open Voltage		1.88	1.98	2.08	V
F_{BM}	Burst Mode Frequency			1/8 F_{OSC}		kHz
Current Sense Input Section (CS pin)						
V_{CST_MAX}	Internal Current Limit Threshold		0.85	0.9	0.95	V
K_{LC}	Line-Sense Current Ratio	I_{LC} / I_{IN}		5		
Line-sense Voltage Section (VIN pin)						
R_{VIN}	VIN Input Resistor		36	45	54	k ohm
V_{UVIN_OFF}	VIN Under-voltage Protection Threshold	R_{IN}=680K,RI=24K	6.2	6.6	7.0	V
V_{UVIN_ON}	VIN Under-voltage Protection Turn-off Threshold	R_{IN}=680K,RI=24K	7.1	7.6	8.1	V
Timing Section						
T_{D_OVP}	VDD OVP Delay Time			200		uSec
T_{D_UVIN}	UVIN Delay Time			200		uSec
T_{D_PL}	FB Pin Open-loop Protection Delay Time	RI=24K		32.5		mSec
T_{RI_SHORT}	RI Pin Short-circuit Protection Detection Time	RI=24K		52		uSec
T_{SLEEP}	Rest Time of FB Pin Open-loop Protection	RI=24K		1.67		Sec

Pin Connection

(TOP VIEW)



Internal Block Diagram



Pin descriptions

Pin No.	Pin Name	I/O	Description
1	VIN	I	Line input voltage sensing, connected to rectified line input source via large value resistor.
2	FB	I	Voltage feedback via opto-coupler for loop regulation. The PWM's duty cycle is generated by the FB voltage and the current sense signal at pin 3 (CS).
3	CS	I	Current sense input.
4	SS	I	Soft-start time setting port. Soft-start time is set by connecting an external capacitor from pin to GND.
5	RI	I	Switching frequency setting with external resistor connected from RI and GND. This pin has short-to-GND protection.
6	GND	P	IC ground.
7	GATE	O	External power MOSFET gate drive output via totem-pole driver .
8	VDD	P	IC power supply.

Typical Performance Curves

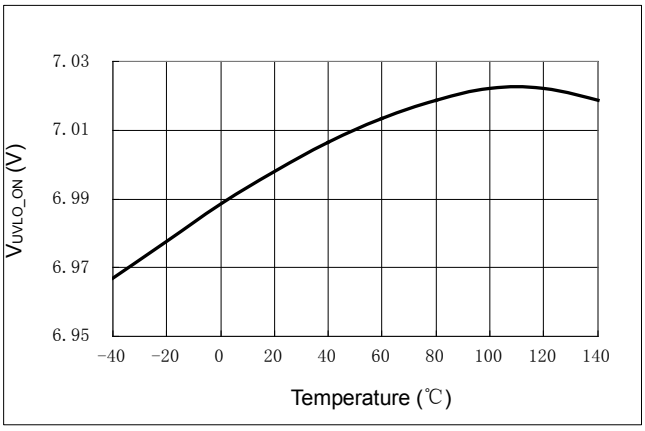


Figure 1 V_{UVLO_ON} VS Temperature

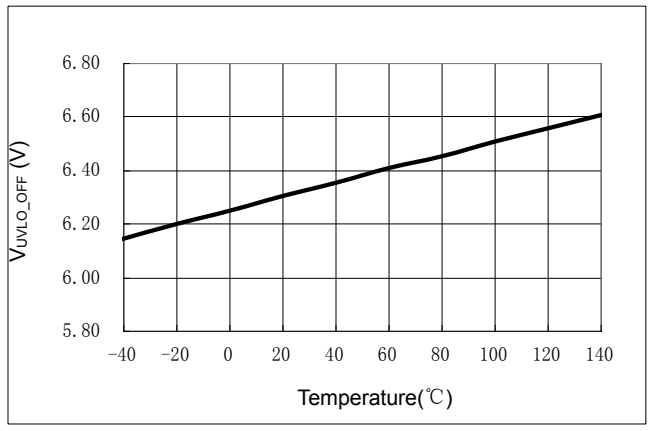


Figure 2 V_{UVLO_OFF} VS Temperature

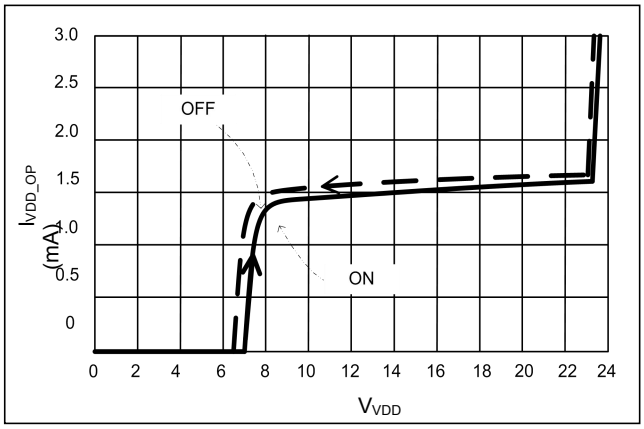


Figure 3 I_{VDD_OP} VS VDD

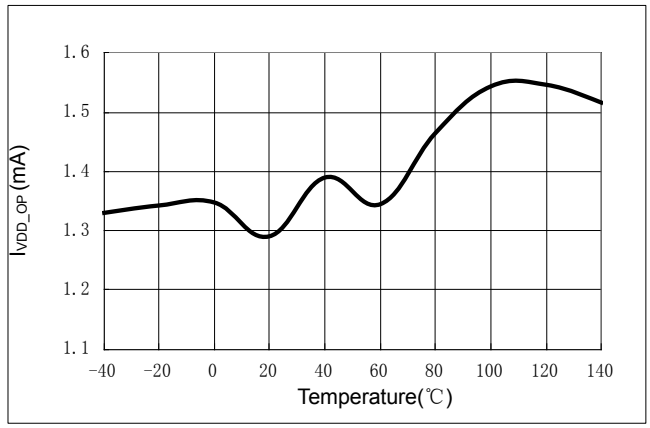


Figure 4 I_{VDD_OP} VS Temperature

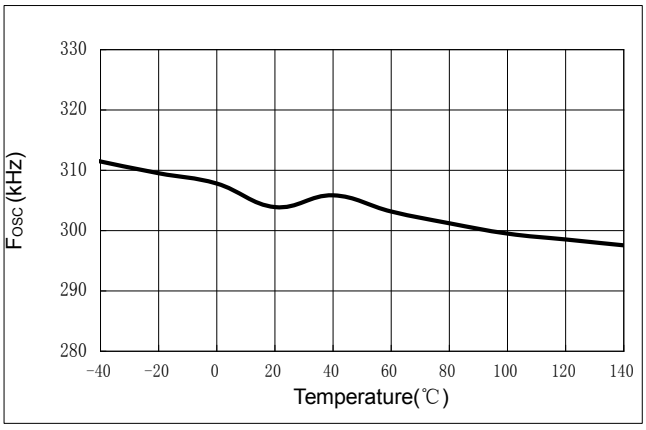


Figure 5 F_{OSC} VS Temperature

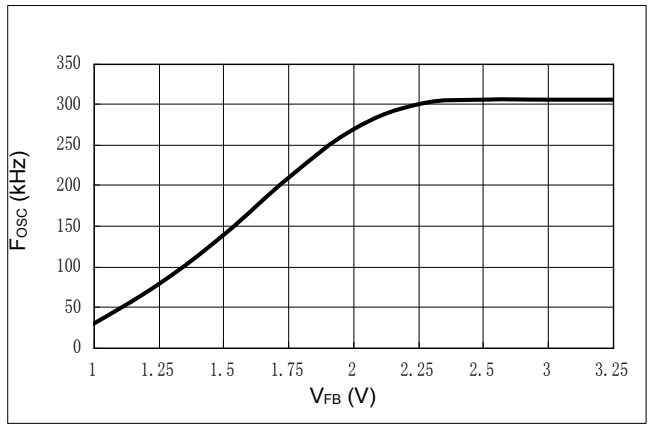


Figure 6 F_{OSC} VS V_{FB}

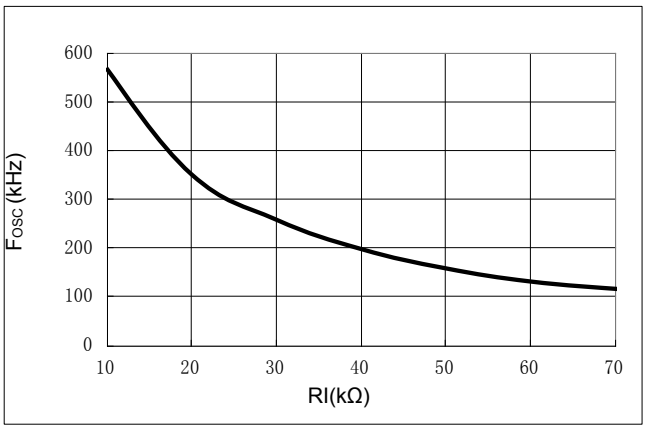


Figure 7 F_{OSC} VS RI

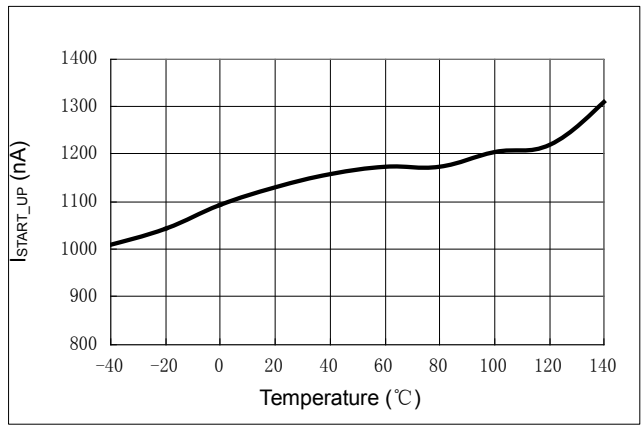


Figure 8 I_{START_UP} VS Temperature

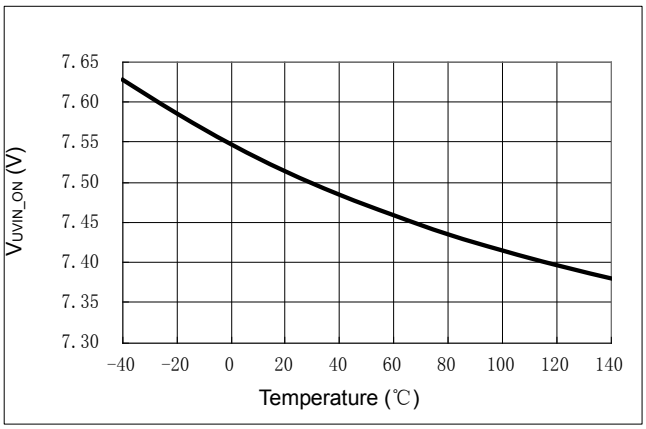


Figure 9 V_{UVIN_ON} VS Temperature

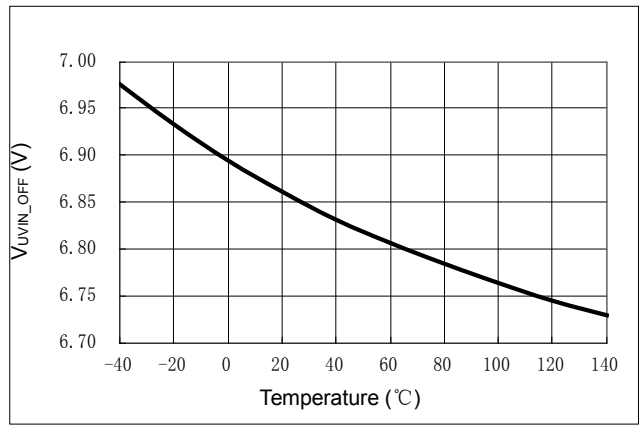


Figure 10 V_{UVIN_OFF} VS Temperature

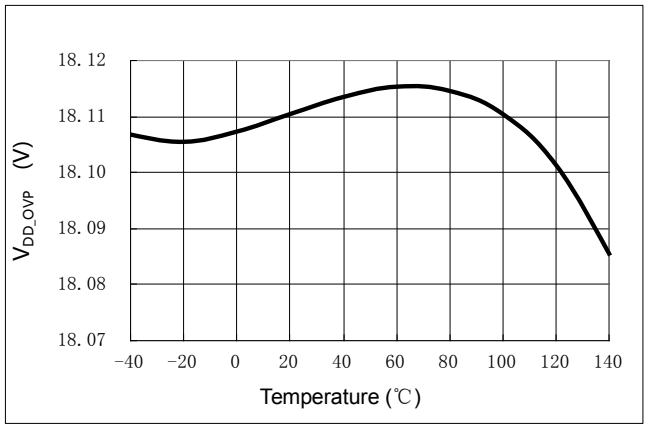


Figure 11 V_{DD_OVP} VS Temperature

(1) Condition: VDD=12V, RI=24kΩ, T_A=25℃ (unless otherwise specified).

(2) The curves UVIN (ON) vs Temperature and UVIN (OFF) vs temperature are measured with RI=24kΩ and Rin=680kΩ.

Functional Description

This highly integrated SCM1101A current mode PWM controller is designed for offline DC-DC converter applications. It's two key features are:

1. Under light load conditions, the IC will automatically reduce the PWM's switching frequency to achieve the highest possible efficiency. When the load is at or close to zero, the system enters into burst mode, thus reducing switching losses in standby operation.

2. Highly integrated protection features save the PCB area by reduced external component count and therefore improved system reliability.

Condition: VDD=12V, RI=24kΩ, TA=25℃ (unless otherwise specified).

Extremely Low Start-up and Operating Current

The typical start-up current of SCM1101A is only about 1uA. This value refers to the chip's current consumption before the VDD voltage reaches the startup threshold voltage of 7.1V. Most of the startup circuit's current is used to charge the VDD capacitor, thus accelerating the start-up time of the chip.

The typical operating current of the SCM1101A part is as low as 1.4mA. The relatively small operating current results in higher efficiency and reduces the required VDD hold-up capacitance value.

Oscillator Frequency

To program the maximum switching frequency, a resistor between RI pin and GND with the following calculated value is being used:

$$F_{max}(kHz) = \frac{7320}{RI(k\Omega)} \quad (1)$$

The recommended operating frequency range of the SCM1101A is between 200kHz and 500kHz (see also recommended operating parameters). If the resistor value connected to RI pin is too large (RI pin may become oversensitive) and the resulting operating frequency is too low. Also note that under extremely light load condition the minimum frequency can be less than 22kHz, resulting in the system generating some audible noise.

If the operating frequency is too high, the power consumption of the chip will increase and the precision of frequency will decrease.

Externally Programmable Soft-start Function

This chip design allows the user for easy programming of the soft-start time Tss by means of connecting a capacitor between the SS pin and GND. The charge current ISS from the SS pin into the capacitor is calculated as follows:

$$I_{ss} = \frac{5}{8RI} \quad (2)$$

The correlation between the VSS voltage on the soft-start capacitor and the FB feedback voltage V_{FB} is:

If value of $V_{FB} \geq V_{SS}$, then V_{FB} is controlled by V_{SS} and V_{FB} signal is following V_{SS};

If value of $V_{FB} < V_{SS}$, then V_{FB} is no longer controlled by V_{SS}.

Describing a soft-start cycle: At the beginning of a converter start-up cycle, there is no current flow from the FB pin into the opto-coupler. The V_{FB} voltage follows the V_{SS} signal that rises as defined by C_{SS}. The duty cycle controlled by the PWM comparator will slowly increase going through the soft-start state. Under normal operation, the optocoupler starts pulling current from the FB port after the voltage feedback loop is established. As V_{FB} drops, V_{SS} signal will continue to climb with a fixed slope up to a maximum value, and the constant maximum value is maintained. This way V_{FB} becomes lower than V_{SS}, and will therefore not be controlled by V_{SS}. The peak current value is controlled by the voltage feedback loop, resulting in a smooth transition of the soft -start control into a feedback control loop operation. In other words, by the time the V_{SS} signal rise settles, the V_{FB} signal has also been established.

In addition, the chip features an integrated soft-start reset function and an SS pin suspending protection function.

Soft-start reset: If the chip's start-up or the self-recovery protection is revoked, the soft-start circuit enters a reset process by first resetting V_{SS} to ground potential, before resetting V_{FB} as well.

SS pin suspending protection: If the SS pin voltage V_{SS} raises after a soft-start reset up to 0.9V in 4us, the system recognizes the SS pin as suspended and will lock the GATE signal to low voltage level, indicating it has entered the SS pin suspending protection state. This protection prevents the device from being damaged by the large peak currents under following start-up conditions: The SS pin is open (not connected to soft-start capacitor, capacitor faulty) or the selected external capacitor value is too small.

Smart Green Mode

The SCM1101A detects the FB port voltage V_{FB} for adjusting the oscillator frequency, which in turn adjusts the output GATE signal frequency. If 2.2V < V_{FB} < 3.8V, the system works in normal PWM mode; only the peak voltage of the CS pin is adjusted, the frequency maintains the maximum value. If 1.3V < V_{FB} < 2.2V, the system works in PWM+PFM mode; both the CS peak voltage and the systems operating frequency are regulated. The switching frequency gradually decreases with decreasing load, and if 1.05V < V_{FB} < 1.3V the system works in PWM mode and it has reached the minimum operating frequency which equals to 1/8 of the maximum operating frequency; when V_{FB} is less than 1.05V, the system enters into the energy saving burst mode with the GATE signal pulled low (see below 12.5). How V_{FB} signal changes influences operating modes is shown in figure 12 below:

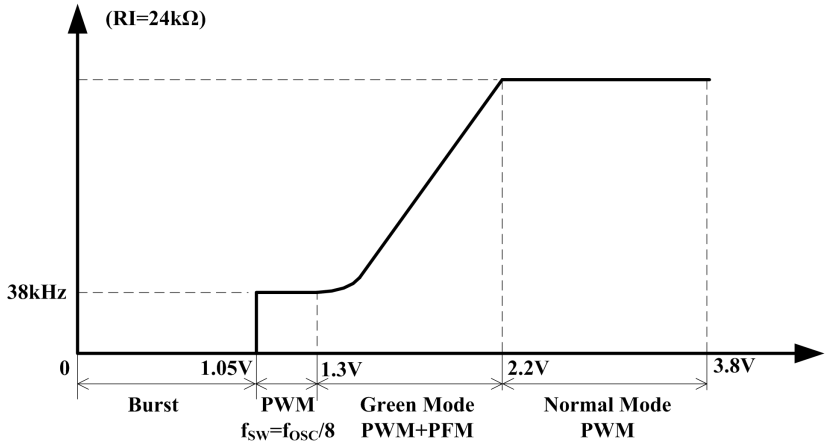


Figure 12 FB pin voltage vs output frequency

Burst Mode

In addition to the Smart Green Mode, a Burst Mode is also part of the SCM1101A design. If the V_{FB} signal decreases to 1.05V, the system enters Burst Mode, which is also known as frequency hopping mode. At this point, the PWM controller stops switching, the output voltage starts to drop according to the power consumption of the load, which causes the opto-coupler current to be reduced and the V_{FB} signal starts to rise again. As soon as the V_{FB} voltage rises above the threshold of 1.1V, the output driver resumes at the minimum switching frequency (i.e., 1/8 of the maximum frequency). In order to avoid any audible noise, the minimum switching frequency should be set higher than 22kHz. After the GATE output resumes to normal, the output voltage starts to rise again. Only when V_{FB} reverses below the 1.05V trigger point again, the system recycles and returns to the burst mode once again, as shown in figure 13.

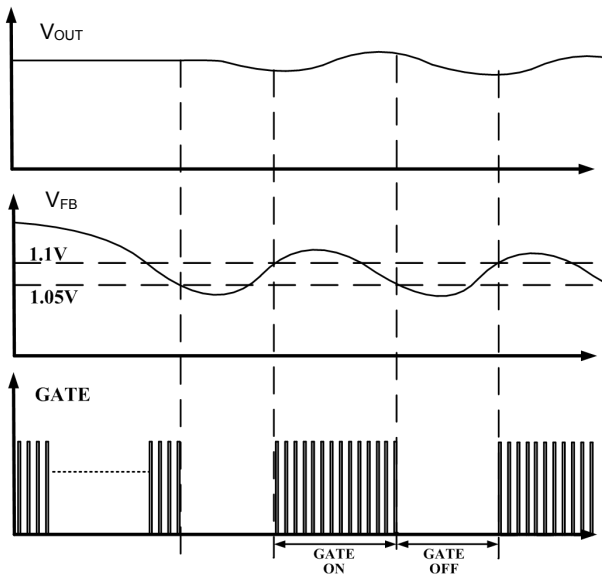


Figure 13 Burst mode time sequence

Feed-forward Compensation

By sampling the input voltage at the VIN pin, the feed forward resistor R_{LC} generates the compensation voltage V_{RLC}, which accomplishes the feed forward compensation and ensures a consistent over current point over the entire input voltage range. The R_{LC} feed forward resistor value can be calculated by the following formula:

$$R_{LC} = \frac{(R_{IN} + 45k\Omega) \times T_D}{5 \times L_P} \times R_{CS} \quad (3)$$

·T_D is the current detection delay time, including the MOSFET turn off delay.
·L_P is the primary side transformer inductance.

·R_{IN}, R_{CS} respectively represent the input resistance and the current sense resistance (see also typical application).

Built-in Slope

The design consists of a two-stage compensation; when the duty is between 44% and 60%, the slope is 194.3mV/us and when the duty cycle is between 60% and 80%, the slope is 322.1mV/us. This two-stage design prevents the slope compensation from affecting the load carrying capacity.

The above mentioned typical slope values are based on an external 24kΩ resistor connected to the RI pin.

Maximum Peak Current Limit

The SCM1101A limits the voltage of the CS pin to V_{CST_MAX} (see electrical characteristics), and the maximum peak current I_{PK_MAX} of the primary side inductance meets the following (slope compensation not taken into account):

$$I_{PK\_MAX} = \frac{0.9 - V_{RLC}}{R_{CS}} \quad (4)$$

V_{RLC} is the voltage on the feed forward resistance mentioned above, calculated as follows:

$$V_{RLC} = \frac{V_{IN} \times T_D}{L_P} \times R_{CS} \quad (5)$$

R_{CS} is the value of current sense resistance.

Limiting the maximum peak current will limit the maximum output current, calculated by the turns ratio. If the load current exceeds the maximum output current, the output voltage will drop sharply, the opto-coupler no longer pulls current from FB port, the V_{FB} value will rise until triggering the V_{FB} overvoltage protection (see below).

VIN Undervoltage Protection

VIN undervoltage protection point: V_{UVIN_OFF} can be set by the input resistor R_{IN}.The chip enters undervoltage protection state when the input voltage is lower than:

$$0.22 \times (R_{IN} + 45) / RI \text{ .}$$

The undervoltage protection is cancelled once the input voltage is greater than:

$$0.25 \times (R_{IN} + 45) / RI$$

resulting in a soft-start cycle being initiated. Note: Use resistor values for R_{IN} and RI in kilo-ohm (kΩ) for above formula.

V_{FB} Overvoltage Protection

Once the accumulated time that the FB port voltage V_{FB} remains above 4.5V exceeds the delay time T_{D_PL} (see electrical characteristics, namely $10240T_{OSC}$,T_{OSC} is minimum switching period time), an overvoltage condition is detected. The chip forces the GATE to turn off immediately going into the V_{FB} overvoltage protection rest state. As long as V_{FB} stays below 4.5V before the elapsed time reaches the T_{D_PL}, the V_{FB} overvoltage protection will not be triggered. T_{SLEEP} is the duration of the V_{FB} overvoltage protection rest state (see electrical characteristics, namely $2^{19}T_{OSC}$). After such a T_{SLEEP} cycle, the V_{FB} overvoltage protection is cancelled and the the GATE signal is re-enabled, while soft-start is being reset pulling V_{FB} down. If the need for protection is no longer present at this time, the chip will run a soft-start cycle.

In similar fashion the V_{FB} overvoltage protection can be used to achieve over-power protection (OPP), output short-circuit protection (OSP) and open-loop protection (OLP), because all these conditions will result in V_{FB} rising to the point where it is exceeding the 4.5V threshold. The following figure shows the sequence of the V_{FB} voltage and the GATE signal under the converters output short-circuit condition. T1 time period represents a soft-start cycle and the V_{FB} signal follows the soft-start capacitor voltage V_{SS}; T2 represents the V_{FB} overvoltage protection delay time during which the GATE signal is still not forced to shut down; T3 represents the rest time of the V_{FB} overvoltage protection; at the end of the T3 phase the system cycles a soft-start reset process before soft-start can resume. If the output short-circuit of fault condition persists, the whole process above repeats itself.

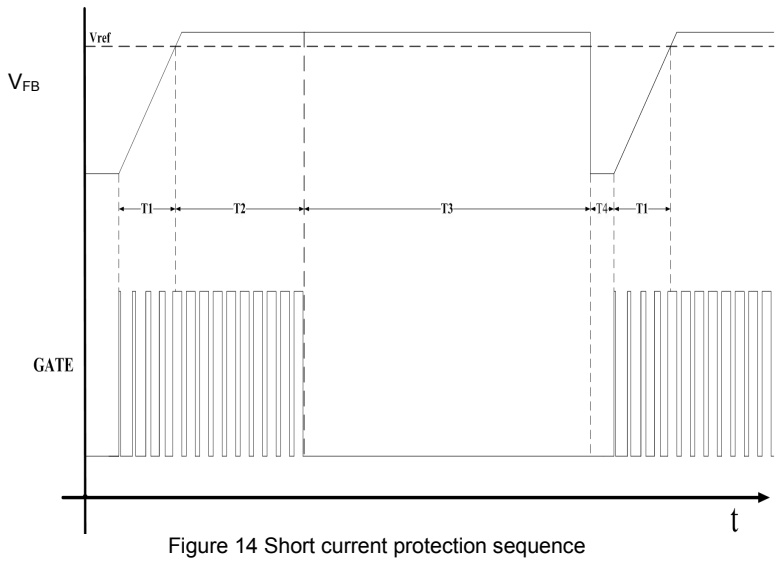


Figure 14 Short current protection sequence

VDD Overvoltage Protection

If the VDD port voltage exceeds 18V (VDD overvoltage protection point) for more than 200us, then the chip enters the VDD over-voltage protection state. The GATE signal stops and only after the VDD voltage decreases below the 14.8V threshold, the chip will cancel the VDD over-voltage protection signal, the soft-start resets, a soft-start cycle is initiated and the GATE signal returns to normal operation.

RI Pin Short-circuit Protection

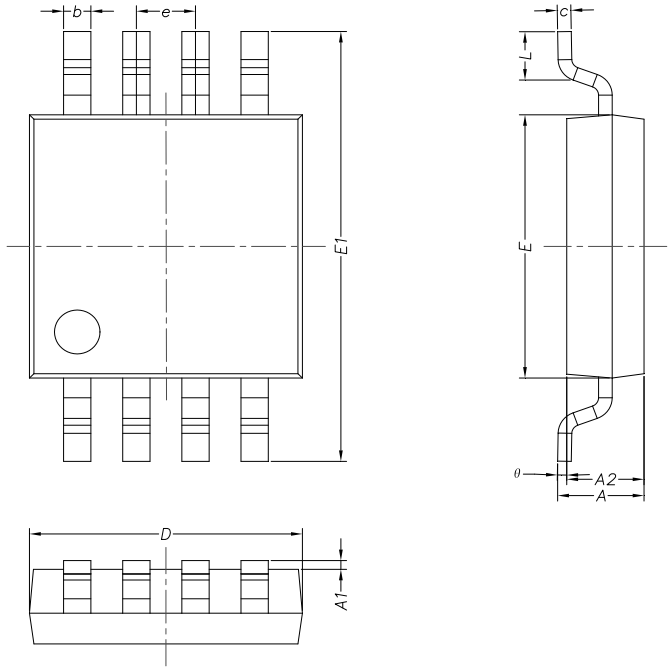
During the protection detection time T_{RI_SHORT} (see electrical characteristics), any RI pin short-circuit condition is being detecting after the chip starts-up. If a short-circuit is detected, the GATE signal stops, the chip will remove the short-circuit protection mode and re-test the condition only when it re-starts again. If there is no short-circuit, it will recognize there is a normal connection on the RI pin, until the chip recycles, restarts and then retests.

Ordering Information

Part number	Package	Number of pins	Product Marking	Tape & Reel	Weight (1 PCS)	Weight (1 REEL include box)
SCM1101AMA	MSOP	8	1101A YM	4K/REEL	0.02g	805.2g

Product marking and date code
SCM1101XYZ:
(1) SCM1101 = Product designation.
(2) X = Version code information (A-Z).
(3) Y = Packaging definition code; S for SOP package,
(4)Z = Operating temperature range (C = 0℃ to +70℃, I =-40℃ to +85℃, A =-40℃ to +125℃, M = -55℃ to +125℃) .
(5) YM = Date code for product traceability; Y = code for production year; M = code for production month.

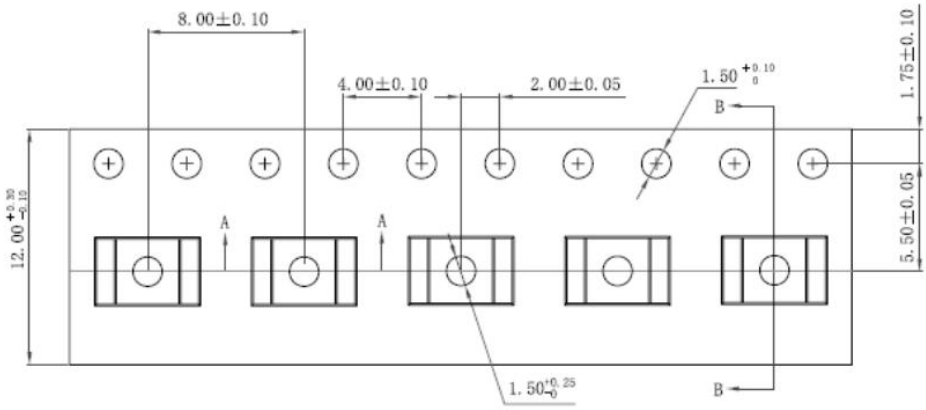
Package Information (MSOP-8)

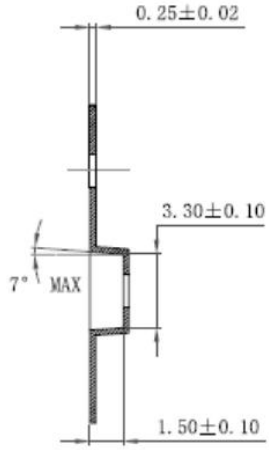


MSOP8				
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

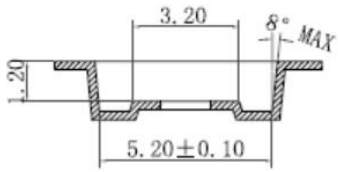
Tape & Reel Information(MSOP-8)

Package	Reel size	Carrier tape	Tape & Reel	Reel/inner box	PCS /inner box	Inner box/outer box	PCS /outer box
MSOP8	13 inch	Pitch=8mm Width=12mm	4000	2	8000	8	64000



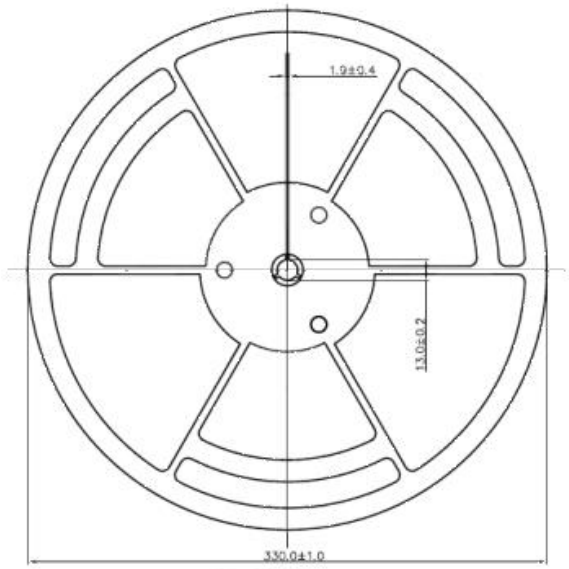


B–B

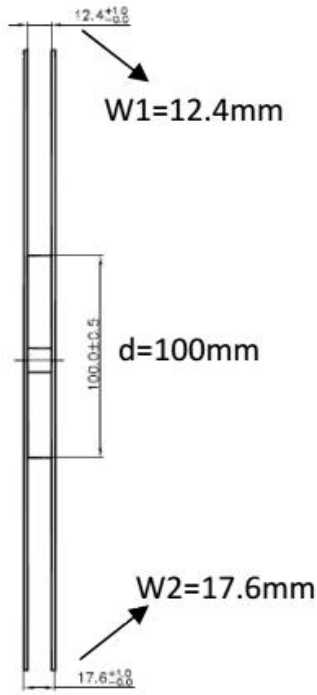


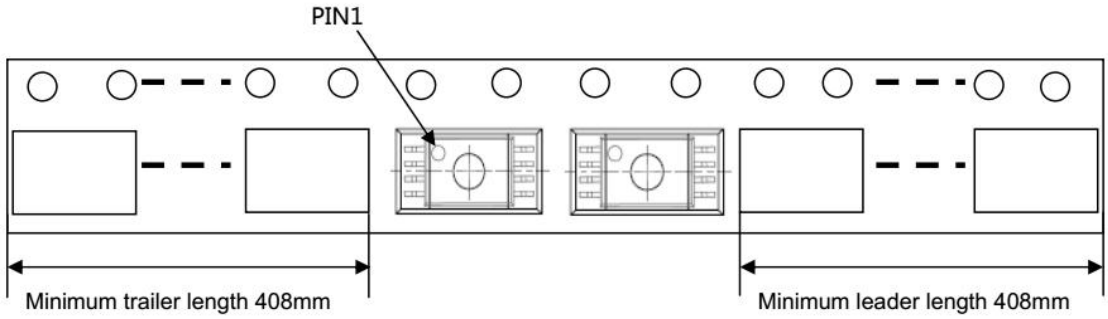
A–A

C



D=330mm





Inner box size（mm）	Outer box size（mm）
565*380*390	360*360*65

Technical requirement：

1. Color：Blue（Reference color number：
   PANTONE DS 196-1 C ; C100 M70 Y0 K0
   PANTONE DS 197-1 C; C100 M70 Y0 K10
   PANTONE DS 205-1 C; C100 M60 Y0 K20
   PANTONE DS 205-2 C; C85 M50 Y0 K20
   PANTONE DS 206-2 C; C85 M50 Y0 K35
   PANTONE DS 219-1 C; C90 M50 Y5 K15)
2. Dimensions and tolerances according to ANSI/EIA-481-C-2003;
3. Disk surface good finish, no warping deformation；
4. External packing in good condition, no damage or pollution;

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