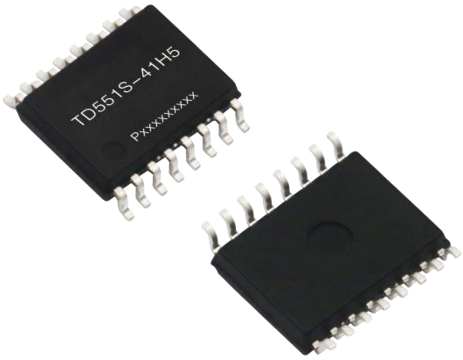
TD551S-4xH5
SOIC package integrated isolated DC-DC converter

Features

- Ultra-small, ultra-thin, chip scale SOIC package
- Baud rate up to 150Mbps
- Wide input supply range: 4.5 V to 5.5 V
- High isolation to 5000Vrms
- Nanosecond propagation delay
- Integrated overload, short-circuit protection and thermal shutdown
- High CMTI: 180 kV/μs (typical)
- Industrial operating ambient temperature range: -40℃ to +125℃
- RoHS-Compliant Packages: SOIC16-WB

Package



Applications

- Bus isolated communication
- Isolated sensor interface
- Industrial automation systems
- Motor control
- Medical isolated
- Test and measurement
- Isolated ADC, DAC

Functional Description

TD551S-4xH5 is a family of high-performance reinforced digital isolators with an integrated isolated DC-DC converter. TD551S-4xH5 eliminate the need for a separate, isolated power supply, which results in a small form factor, total isolation solution.

TD551S-41H5 device has three forward and one reverse-direction channels, TD551S-42H5device has two forward and two reverse-direction channels, and it has fail-safe mode option. If the input signal is lost, default output is low for devices with H. .

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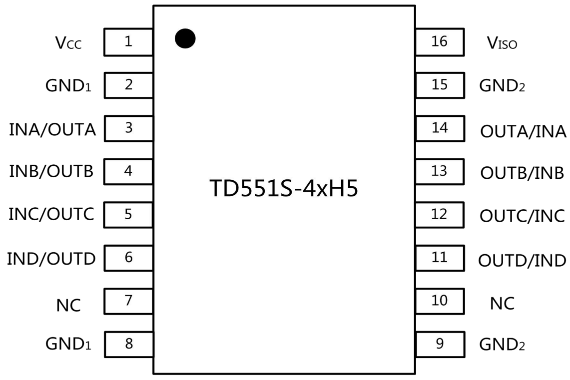
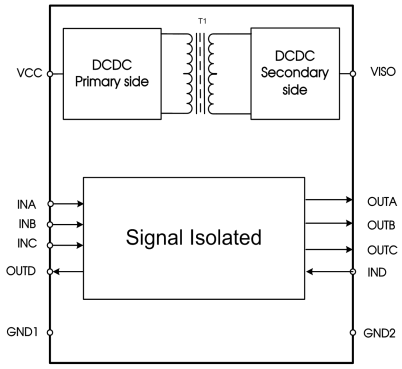
Pin Connection



Note：All GND1 pins are not internally connected;
All GND2 pins are not internally connected.

Internal Block Diagram



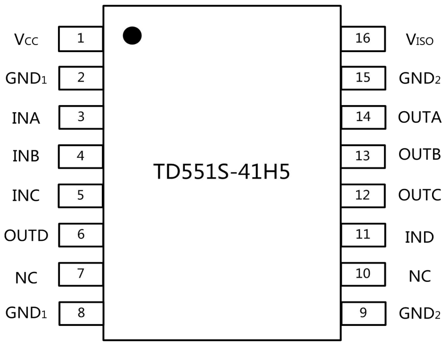
Function Table

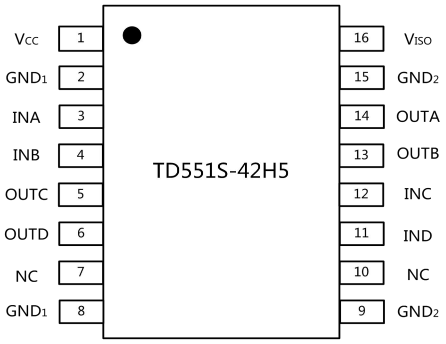
Table 1. Operation Mode Table

V_{CC}	Input	Output	Operation
PU	H	H	Normal operation mode: A channel’s output follows the input state
	L	L	
	Open	Default	Default output fail-safe mode: If a channel’s input is left open, its output goes to the default high level.
PD	X	Undetermined	

Note:
PU = Powered up ; PD = Powered down; X = Irrelevant; H = High level; L = Low level.

Pin Descriptions





Pin Number	Pin Name	Pin Functions
1	V_{CC}	Power supply(Side 1) By using 0.1uF and 22uF ceramic capacitance GND_1
2	GND_1	Ground(Side 1)
3	INA	Digital input(Side 1)
4	INB	Digital input(Side 1)
5	INC/OUTC	Digital input/output(Side 1)
6	OUTD	Digital output(Side 1)
7	NC	No Connect.
8	GND_1	Ground(side 1)
9	GND_2	Ground(Side 2)
10	NC	No Connect.
11	IND	Digital input(Side 2)
12	OUTC/INC	Digital output/input(Side 2)
13	OUTB	Digital output(Side 2)
14	OUITA	Digital output(Side 2)
15	GND_2	Ground(Side 2)
16	V_{ISO}	Isolated output supply voltage determined by SEL pin. By using 0.1uF and 47uF ceramic capacitance Ground2.

Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (unless otherwise specified).

Parameters	Unit
Supply voltage V_{CC}	-0.4V to +6V
Input voltage V_{in}	-0.5V to V_{CC}+0.5V
Output current I_O	-15mA to +15mA
Receiver Output current T_J	< 150℃
Operating temperature range	-40°C to +125°C
Storage temperature range	−65°C to +150°C

Important: Exposure to absolute maximum rated conditions for an extended period may severely affect the device reliability, and stress levels exceeding the “Absolute Maximum Ratings” may result in permanent damage.

Recommended Operating Conditions

Parameters			Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.5		5.5	V
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
I_{OH}	High-level Output Current	V_{CCO}=5V	-4			mA
I_{OL}	Low-level Output Current	V_{CCO}=5V			4	mA
T_A	Ambient Temperature		-40		125	°C
P_D	Maximum Power Dissipation	V_{CC}= 5.5V, I_{LOAD}=100mA, all digital channels input :f=75MHz ; Duty=50%		1.0	1.48	W
DR	Data Rate		0		150	Mbps

Note: V_{CCI} = signal input side supply; V_{CCO} = signal output side supply.

Electrical Characteristics

General test conditions and V_{CC}=V_{IO}= 5V, Ta = 25℃ (unless otherwise specified).

V_{CC}= 5 V ± 10%, T_A= -40 to 125°C

Parameters		Conditions	Min.	Typ.	Max.	Unit
V_{ISO}	Isolated supply voltage	External I_{ISO}=0 to 50mA	4.75	5.07	5.25	V
		External I_{ISO}=0 to 100mA	4.5	5.07	5.25	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO}=50mA, Input voltage change ±1%			1.5	mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO}=0 to 100mA		2		%
EFF	Efficiency at maximum load current	I_{ISO}=100mA , C_L=0.1uF||10uF ; V_I=0V		53		%
$V_{CC(UVLO+)}$	V_{CC} under voltage threshold when supply voltage is rising				4.5	V
$V_{CC(UVLO-)}$	V_{CC} under voltage threshold when supply voltage is falling		2.1			V
$V_{HYS(UVLO)}$	V_{CC} under voltage threshold hysteresis			0.2		V
I_{IH}	High-level input leakage current	V_{IH}=VCCI at INx			20	uA
I_{IL}	Low-level input leakage current	V_{IL} = 0V at INx	-20			uA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, Figure 8	V_{CCO} – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, Figure 8		0.2	0.4	V
CMTI	Common-mode transient immunity	V_I = 0 V or VCC, Figure 9		180		kV/us
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)			50		mV

Supply Current Characteristics

V_{CC}= 5 V ± 10%, T_A= -40 to 125°C

Parameters		Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Current drawn from supply	No external I_{LOAD} ; V_I=0V		16	30	mA
		No external I_{LOAD} ; V_I=V_{CCI}		12	24	
		All channels switching : f=1Mbps, Duty=50%; C_L=15pF, No external I_{LOAD}		17		
		All channels switching : f=10Mbps, Duty=50%; C_L=15pF, No external I_{LOAD}		20		
		All channels switching : f=100Mbps, Duty=50%; C_L=15pF, No external I_{LOAD}		35		

Note:

1.V_{CCI} = signal input side supply; V_{CCO} = signal output side supply.

2.When T_A > 105℃, Current available to isolated supply should be reduced by 2.5mA/℃.

Transmission Characteristics

General test conditions and V_{CC}=V_{IO}= 5V, Ta = 25℃ (unless otherwise specified).

Parameters		Conditions	Min.	Typ.	Max.	Unit
DR	Data Rate		0		150	Mbps
PW_{minL}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Figure 8		10.0	15.0	ns
PWD	Pulse Width Distortion | t_{PLH} - t_{PHL} |			0.2	4.5	ns
$t_{rk(O)}$	Channel-to-channel Output Skew Time			0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time			2.0	4.5	ns
t_r	Output Signal Rise Time	Figure 8		2.5	4.5	ns
t_f	Output Signal Fall Time			2.5	4.5	ns

Note:

1.$t_{rk(o)}$ is the skew between outputs of a single device with all driving inputs connected and the outputs switching in the same direction while driving identical loads.

2.$t_{rk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

Physical Specifications

Parameters	Value	Unit
Weight	0.4(Typ.)	g

Test Circuits

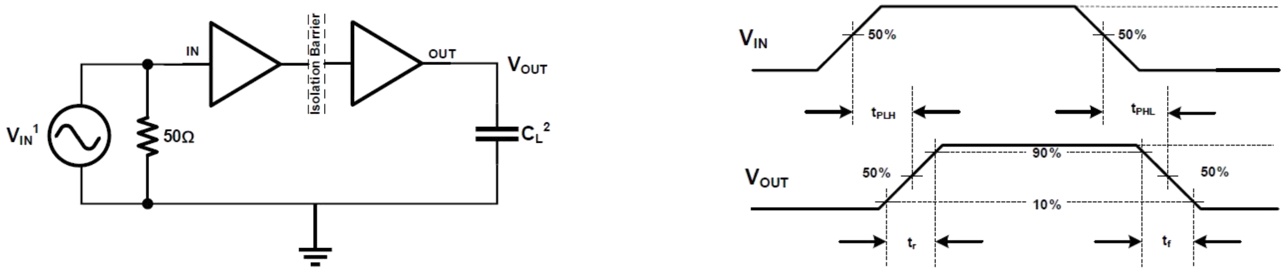


Figure 8. Timing Characteristics Test Circuit and Voltage Wave forms

Note:

1. A square wave generator generate the VIN input signal with the following constraints: waveform frequency ≤ 100kHz, 50% duty cycle, $t_r \leq$ 3ns, $t_f \leq$ 3ns. Since the waveform generator has an output impedance of Z_{out} = 50Ω, the 50Ω resistor in the figure is used for matching. There is no need in the actual application.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

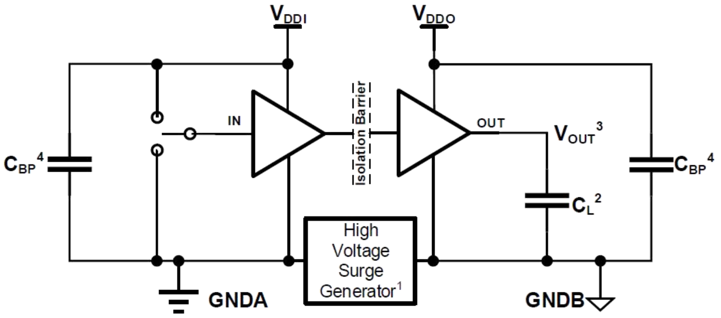


Figure 9. CMTI Test Circuit

Note:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1.5kV amplitude and <10ns rise time and fall time to reach common-mode transient noise with > 150kV/μs slew rate.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance.
3. Pass-fail criteria: The output must remain stable whenever the high voltage surges come.
4. C_{BP} is the 0.1 to 1uF bypass capacitance.

Detailed Description

TD551S-4xH5 has a high-efficiency, low-emissions isolated dc-dc converter, with high-speed isolated data channels.

The high-speed isolated data channels use a simple ON-OFF keying (OOK) modulation scheme to transmit signal across the SiO2 isolation capacitors that provide a robust insulation between two different voltage domain and act as a high frequency signal path between the input and the output. The transmitter (TX) modulates the input signal onto the carrier frequency, that is, TX delivers high frequency signal across the isolation barrier in one input state and delivers no signal across the barrier in the other input state. Then the receiver rebuilds the input signal according to the detected in-band energy. The capacitor-based signal path is fully differential to maximize noise immunity, which is also known as common-mode transient immunity. The capacitively-coupled architecture provides much higher electromagnetic immunity compared to the inductively coupled one.

Application circuit

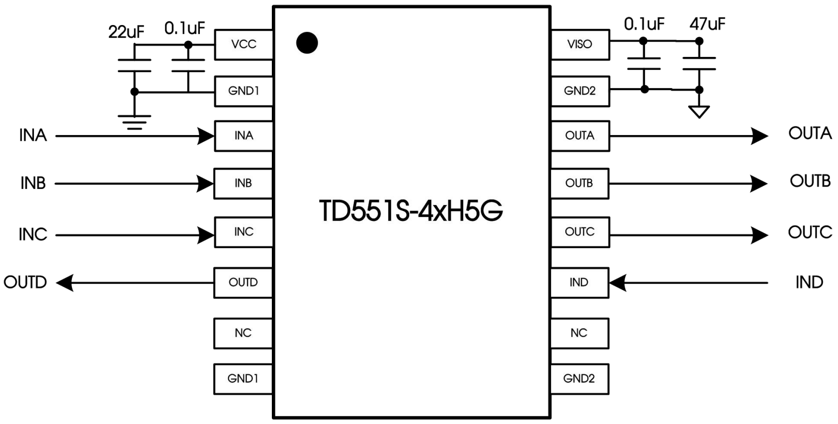
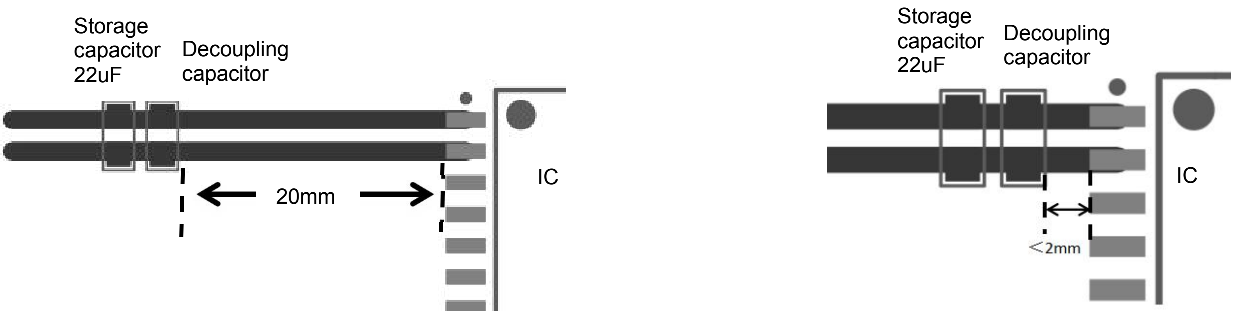


Figure10. Typical application

PCB Design Instructions

1. The decoupling capacitors and energy storage capacitor of VCC and GND1, VISO and GND2 should be placed as close the chip pins as possible to the chip pins to reduce loop area and parasitic inductance of PCB traces. General control should be within 2mm. The decoupling capacitor is placed close the chip, and the energy storage capacitor is placed outside. As shown in Figre10-1.

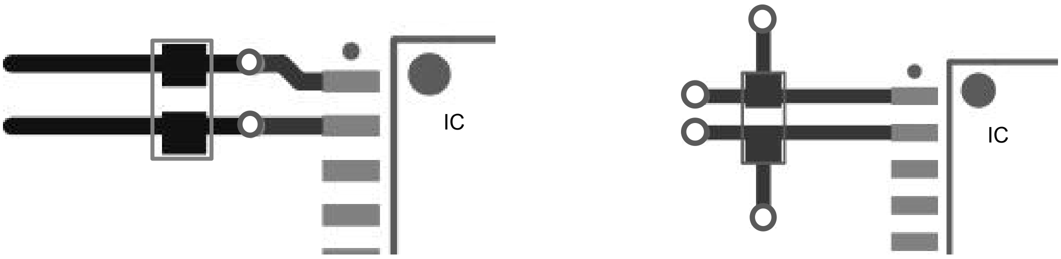


Not recommended

Recommend

Figure10-1

2. The power line width should be designed at least 0.5mm when wiring.
3. When it is necessary to place vias in the power supply line and the ground wire, the position of the vias should be placed on the outside of the capacitor relative to the chip pins ,rather than between the capacitor and the chip, as shown in the figure10-2 below to reduce the number of vias effect of parasitic inductance.



Not recommended

Recommend

Figure10-2

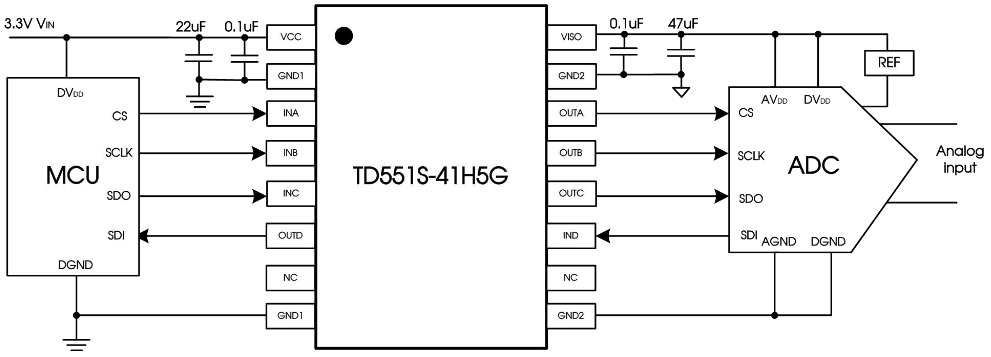


Figure11. Isolated Power and SPI for ADC Sensing Application with TD551S-4xH5

Design requirement:

Parameter	Value
Input voltage V_{IN}	4.5V to 5.5V
Decoupling capacitors between V_{CC} and GND1	0.1uF, 22uF
Decoupling capacitors between V_{ISO} and GND2	0.1uF, 47uF

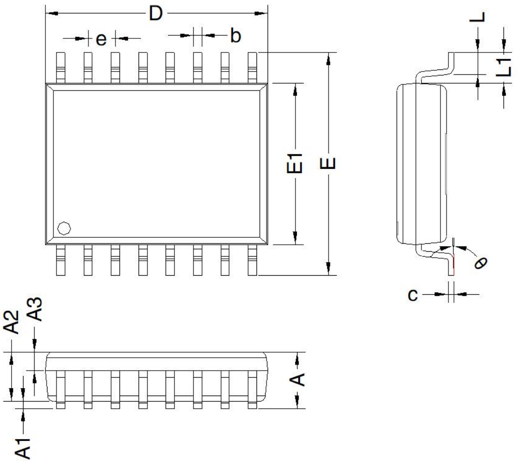
Because of the higher current flowing though the VCC and VISO power supplies of TD551S-4xH5, higher decoupling capacitors usually provide better noise and ripple performance. Although a 10uF capacitor is enough to ensure the normal operation of the product, it is still strongly recommended to use a higher decoupling capacitor(such as 22uF, 47uF) on both VCC and VISO pins to the respective grounds to achieve the best performance.

Ordering Information

Part number	Package	Number of pins	Product marking	Tape & Reel
TD551S-41H5	SOIC	16	TD551S-41H5	340/REEL
TD551S-42H5	SOIC	16	TD551S-42H5	340/REEL

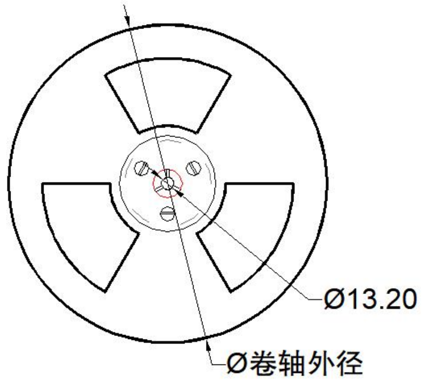
Package Information

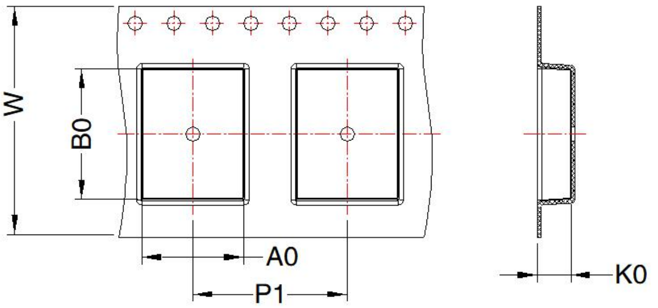
第三角投影

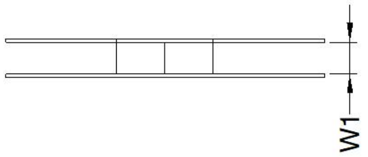


标识	尺寸(mm)	
	Min	Max
A	–	2.65
A1	0.10	0.30
A2	2.25	2.35
A3	0.97	1.07
b	0.35	0.43
c	0.24	0.29
D	10.20	10.40
e	1.27 BSC	
E	10.10	10.50
E1	7.40	7.60
L	0.55	0.85
L1	1.40 BSC	
θ	0°	8°

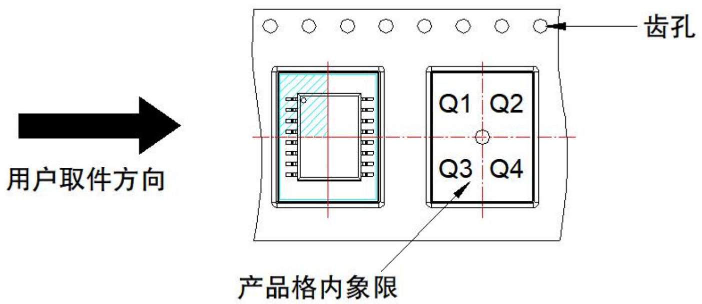
Tape & Reel Information







PIN 1在载带上的象限位置



器件型号	封装类型	Pin	MPQ	卷轴外径 (mm)	卷轴宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限
TD551S-41H5	SOIC16	16	340	180	16.4	10.74	10.65	3.5	16.0	16.0	Q1
TD551S-42H5											

MORNSUN Guangzhou Science & Technology Co., Ltd.

Address: No. 8 Nanyun 4th Road, Huangpu District, Guangzhou, China

Tel: 86-20-38601850 Fax: 86-20-38601272 E-mail: info@mornsun.cn www.mornsun-power.com