MORNSUN®

SCM3510A Dual Channel Bootstrap Driver

Features

- Up to 700V withstand voltage
- 40ns typical propagation delay
- Low quiescent current and operating current
- Wide operating temperature: -40°C~125°C
- Maximum rising and falling time: 15ns
- Dual channel under voltage lockout
- Compatible with 3.3V and 5V input logic
- Up to 100V/ns dV/dt immunity
- Pin compatible with common half-bridges IC in the industry
- Channel matching delay(less than 7ns)

Package

Mechanical package:LGA4x4-10L
(see "Ordering information" for details).

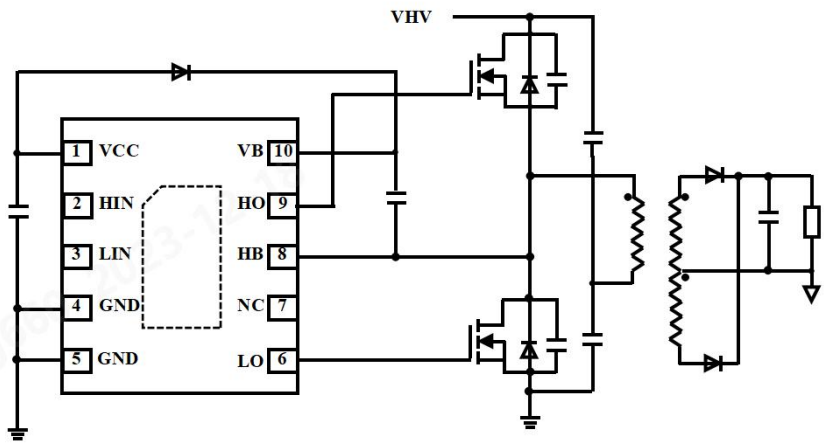
Applications

- High-density SMPS for server, telecommunication and industry
- Half-bridge, full-bridge and LLC converter
- Active clamp flyback/forward converter
- Solar inverter, Motor control
- Electric power steering system

Functional Description

SCM3510A is a high and low sides gate driver which can shift the logic pulse signals received by the HIN and LIN pins to the voltage domain of V_{HB}~V_{VB}, and then output the corresponding driving signals through the HO, LO pins to control the switch of high and low sides power transistors. In high-voltage bootstrap applications, the pulse signals received by HIN and LIN pins of SCM3510A generally come from the main control chip. The main control chip outputs a duty cycle signal based on the loop control to SCM3510A and then SCM3510A restores the duty cycle signal at the HO and LO pins to control the switch of high and low side power transistors.

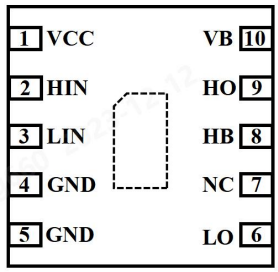
Typical Application Circuit



SCM3510A Typical Application Circuit

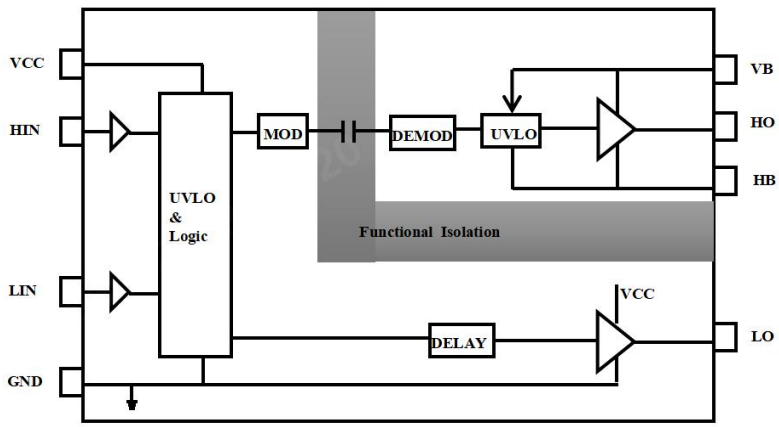
CONTENT

Pin Package



SCM3510A LGA4x4-10L Pin Package

Internal Block Diagram



SCM3510A Simplified Circuit Principles

Pin Description

Pin Name	Functional Description	
1	VCC	IC supply voltage
2	HIN	High side signal input
3	LIN	Low side signal input
4、5	GND	IC reference ground
6	LO	Low side driver output
7	NC	Not connected

8	HB	Negative supply of high side driver
9	HO	High side driver output
10	VB	Positive supply of high side driver

Absolute Maximum Ratings

General test conditions: Ventilation, normal operating temperature range (unless otherwise specified).

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage V_{CC}	-0.3	33	V
LIN, HIN	Input signal voltage	-5	V_{CC}+0.3	V
V_B	Voltage of positive supply of high side driver	-0.3	720	V
V_{HO}	Voltage of High side driver output	V_{HB}-0.3	V_B+0.3	V
V_{LO}	Voltage of Low side driver output	-0.3	V_{CC}+0.3	V
T_{STG}	Storage temperature	-55	150	°C
-	Reflow temperature	-	260	°C
T_J	Junction temperature	-	150	°C
dV_{HB}/dt	Rate of V_{HB} pin change	-	±100	V/ns
ESD	HBM	-	±4000	V
	CDM	-	±1500	V

NOTE:

1.If the stress values listed in the "absolute maximum ratings" table are exceeded, it may cause permanent damage to the devices. Long term operating under extreme rated conditions may affect the reliability of the devices. All voltage values are based on GND reference.

2.This series of ICs include ESD protection and is tested using the following methods: ①The ESD human body model is tested according to AEC−Q100−002 (EIA/JESD22−A114). ②The electrostatic discharge test of charged device model(CDM) is carried out in accordance with AEC−Q100−11 (EIA/JESD22−C101E).③Latchup maximum current ≤150 mA , according to JESD78F.

Recommended Operating Conditions

Symbol	Parameter Description	Min	Max	Unit
V_{CC}	Supply voltage	7	25	V
V_B-V_{HB}	High side supply floating voltage	7	25	V
V_{HB}	Negative voltage of high side driver supply	-1	700	V
V_{HO}	Voltage of High side driver output	V_{HB}	V_B	V
V_{LO}	Voltage of Low side driver output	GND	V_{CC}	V
V_{LIN} , V_{HIN}	Input voltage of high side or low side	GND	V_{CC}-2	V
T_A	Operating temperature	-40	125	°C

Thermal Characteristics

Symbol	Parameter Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance(LGA4x4-10L)[1]	162	°C/W

NOTE:

1.The test values are based on a 50mm^2 copper area with a thickness of 1oz and an FR4 board. Standard JESD51-3 Low Effective Thermal Conductivity Test Board(1s) , in an environment described inJESD51-2a.

Electrical Characteristics

T_A= –40~+125°C. V_{CC} =V_B=12V, V_{HB}=GND, No load, typical values are at Ta=25℃,(unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Supply Characteristics						
I_{CCQ}	V_{CC} Quiescent Current	V_{LIN}=V_{HIN}=0V	-	0.5	0.6	mA
I_{CCO}	V_{CC} Operating Current	f=500kHz, C_{load}=0	-	2.25	2.75	mA
I_{BQ}	High side supply	V_{LIN}=V_{HIN}=0V	-	0.9		mA
I_{BO}	High side supply quiescent current	f=500kHz, C_{load}=0	-	2.75	3.35	mA
I_{IHB}	HB to GND quiescent current	V_{HB} =700V	-	-	0.01	μA
Input Characteristics						
V_{HIT}	Input Rising Threshold	-	2.1	2.7	3.1	V

V_{LIT}	Input Falling Threshold	-	1	1.4	1.8	V
V_{HI_HYS} V_{LI_HYS}	Input Voltage Hysteresis	-	-	1.3	-	V
R_{IN}	Input Pull down Resistance	V_{XIN}=5V	100	175	250	kΩ
Output Characteristics						
$T_{startup}$	High Side Startup Time	Time from V_B>UVLO to the first rising edge of the HO pulse	-	-	30	μs
Driving Characteristics						
V_{OL}	Logic Low Output Voltage	I_{OSNK}=-100mA	-	0.06	-	V
V_{OH}	Logic High Output Voltage	I_{OSRC}=100mA, V_{OH}=V_{CC}−V_{LO}	-	0.12	-	V
R_{OL}	Logic Low Output Resistance	I_{OSNK}=-100mA	-	0.6	-	Ω
R_{OH}	Logic Low Output Resistance	I_{OSRC}=100mA, V_{OH}=V_{CC}−V_{LO}	-	1.2	-	Ω
I_{OSRC}	Peak Source Current	V_O=0V	-	4	-	A
I_{OSNK}	Peak Sink Current	V_O=12V	-	6	-	A
Output Rising/Falling Time						
T_R	LO, HO rising time	C_{load}=1nF(10% to 90%)	-	8	15	ns
T_F	LO, HO falling time	C_{load}=1nF(90% to 10%)	-	8	15	ns
Channel Matching Delay						
T_{MON}	LI ON, HI OFF	Pulse width=1μs	-	-	7	ns
T_{MOFF}	LI OFF, HI ON	Pulse width=1μs	-	-	7	ns
Minimum Pulse Width						
PW_{min}	minimum pulse width	C_{load}=0	-	-	35	ns
Propagation Delay						
T_{DLRR}	LI to LO Turn-on delay	C_{load}=0, Minimum switch Time 50ns	-	40	50	ns
T_{DLFF}	LI to LO Turn-off delay	C_{load}=0, Minimum switch Time 50ns	-	40	50	ns
T_{DHRR}	HI to HO Turn-on delay	C_{load}=0, Minimum switch Time 50ns	-	40	50	ns
T_{DHFF}	HI to HO Turn-off delay	C_{load}=0, Minimum switch Time 50ns	-	40	50	ns

SCM3510A(LGA4x4-10L)

Under voltage Lockout Characteristics						
V_{CCon}	V_{CC} UVLO Rising Threshold	-	5.6	6.25	6.9	V
V_{CCoff}	V_{CC} UVLO Falling Threshold	-	5.1	5.75	6.4	V
V_{CChys}	V_{CC} UVLO Hysteresis Voltage	-	-	0.5	-	V
V_{Bon}	V_B UVLO Rising Threshold	-	5.6	6.25	6.9	V
V_{Boff}	V_B UVLO Falling Threshold	-	5.1	5.75	6.4	V
V_{Bhyst}	V_B UVLO Hysteresis Voltage	-	-	0.5	-	V

Truth Table

Number	Input		Output	
	HIN	LIN	HO	LO
1	0	0	0	0
2	1	0	1	0
3	0	1	0	1
4	1	1	1	1
5	0	x	0	0
6	1	x	1	0
7	x	x	0	0
8	x	0	0	0
9	x	1	0	1

NOTE:x=floating

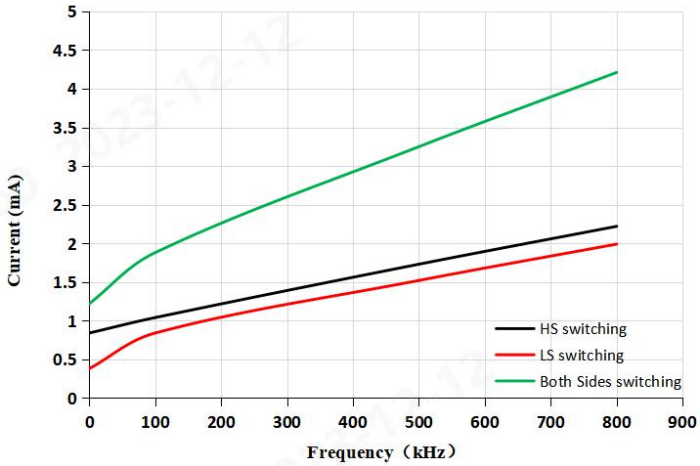


Figure 1 Supply Current I_{CC} VS Frequency (No Load, V_{CC} = 12V)

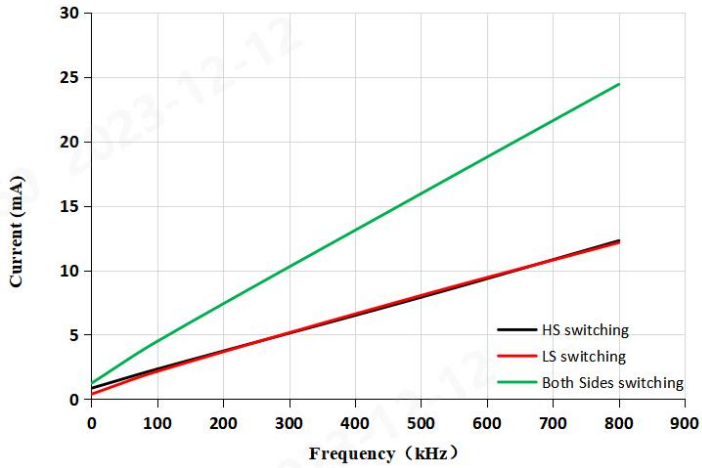


Figure 2 Supply Current I_{CC} VS Frequency(1nF Load, V_{CC} = 12V)

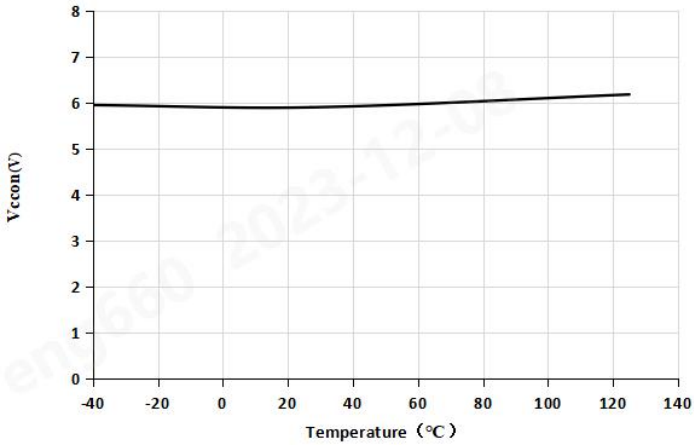


Figure 3 V_{CCon} VS Temperature

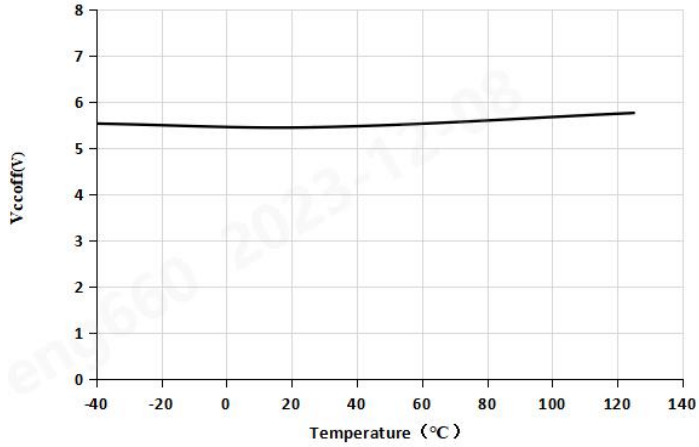


Figure 4 V_{CCoff} VS Temperature

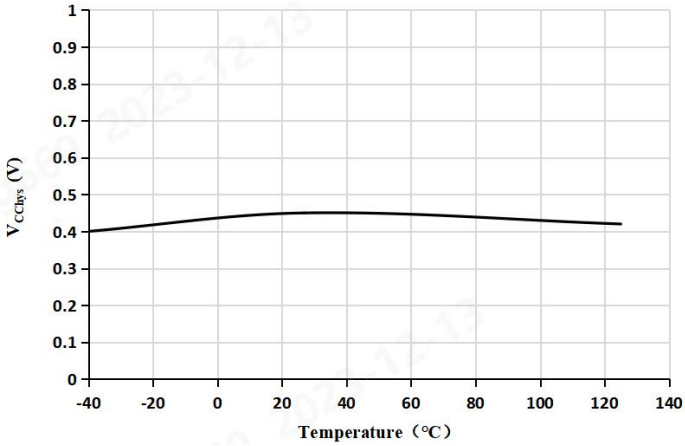


Figure 5 V_{CChys} VS Temperature

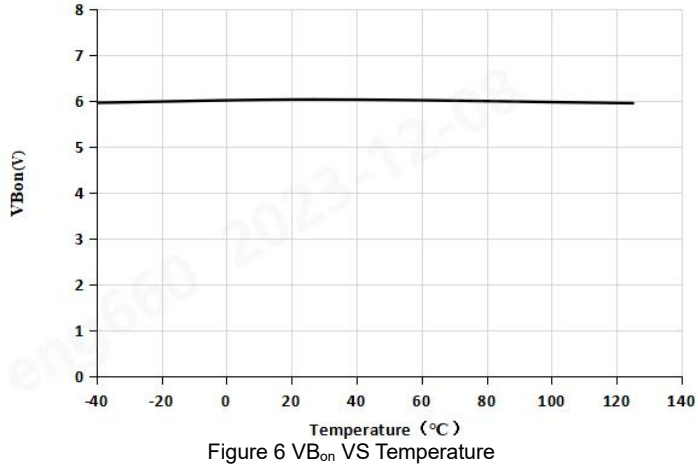


Figure 6 VB_{on} VS Temperature

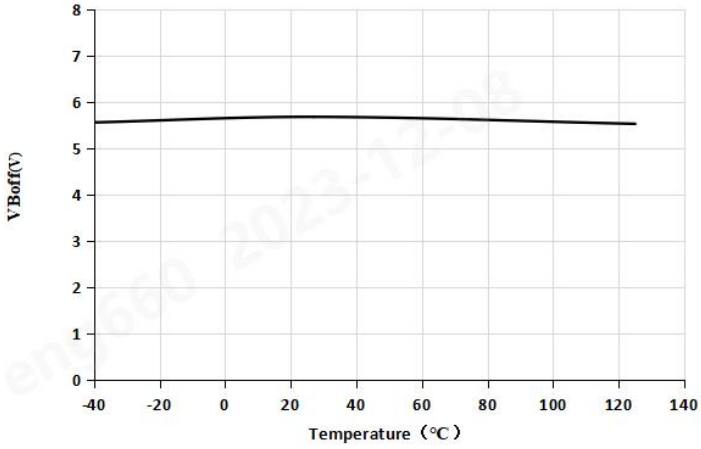


Figure 7 VB_{off} VS Temperature

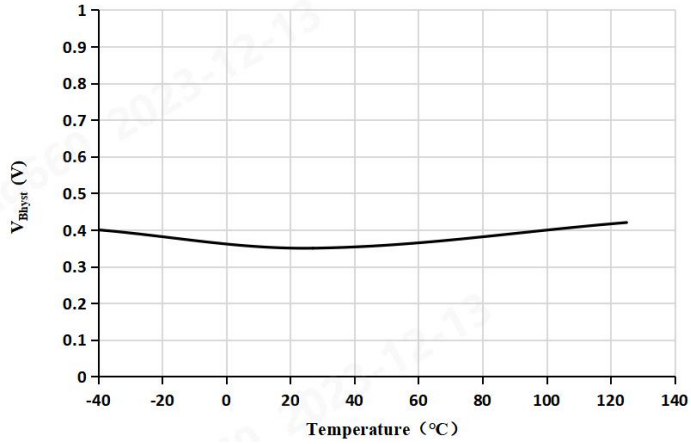


Figure 8 VB_{hyst} VS Temperature

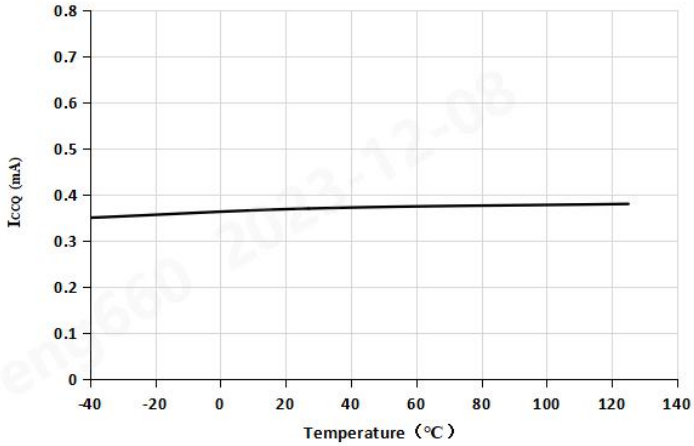


Figure 9 I_{CCQ} VS Temperature

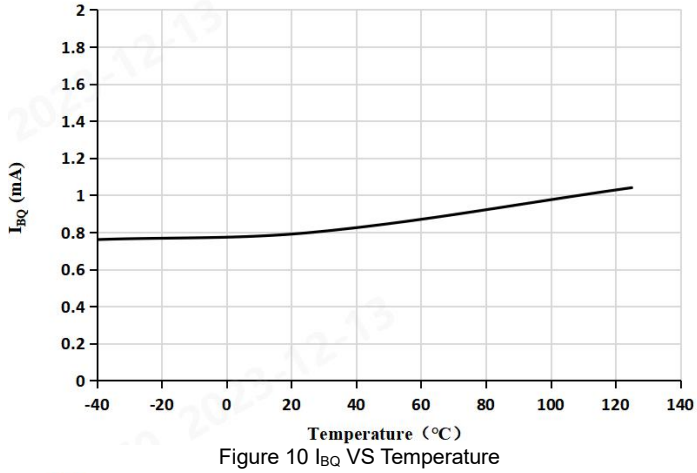


Figure 10 I_{BQ} VS Temperature

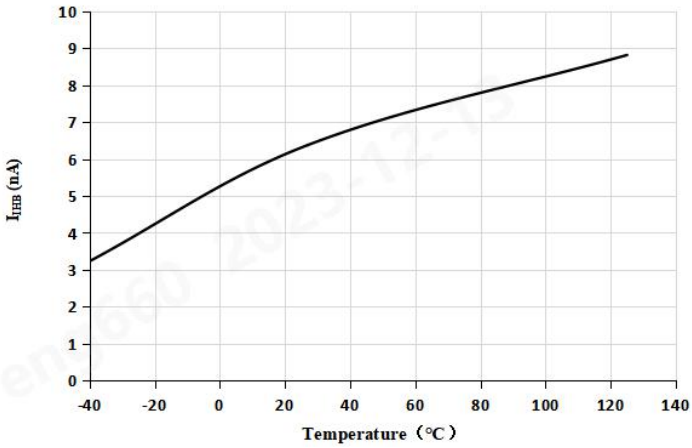


Figure 11 I_{IHB} VS Temperature

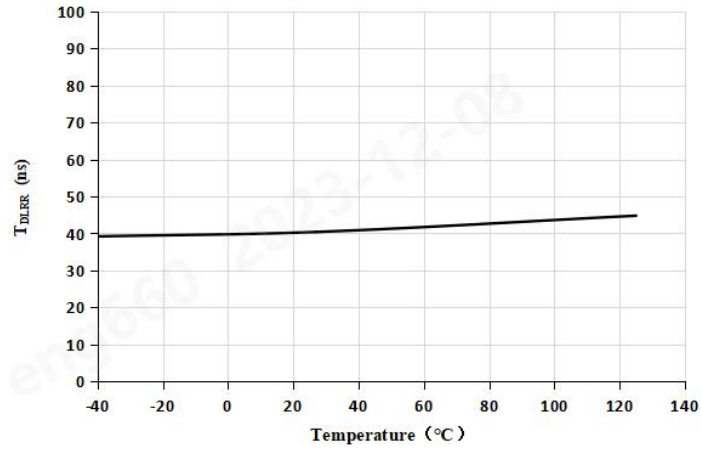


Figure 12 LO Turn-on Propagation Delay VS Temperature

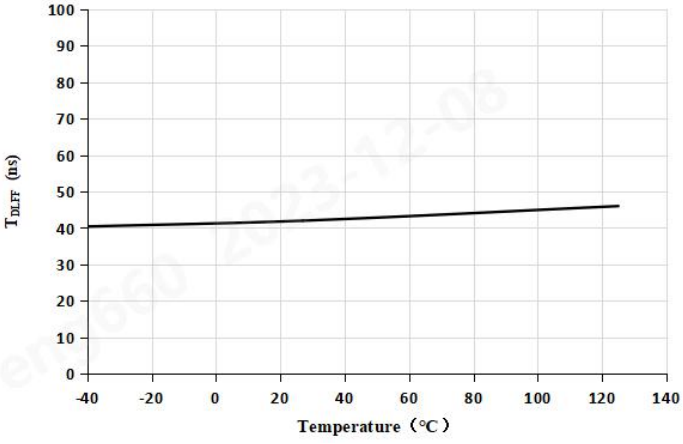


Figure 13 LO Turn-off Propagation Delay VS Temperature

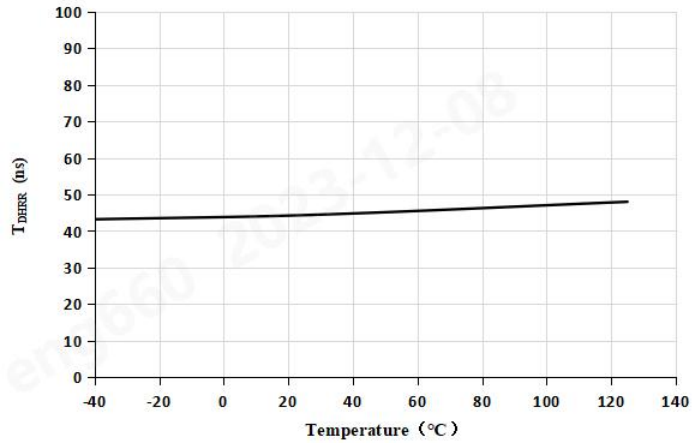


Figure 14 HO Turn-on Propagation Delay VS Temperature

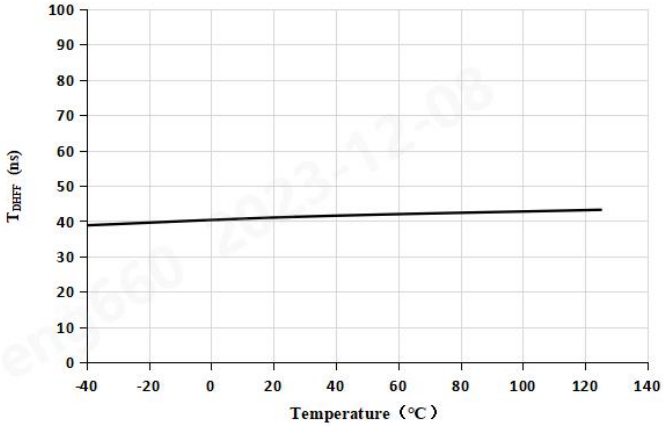


Figure 15 HO Turn-off Propagation Delay VS Temperature

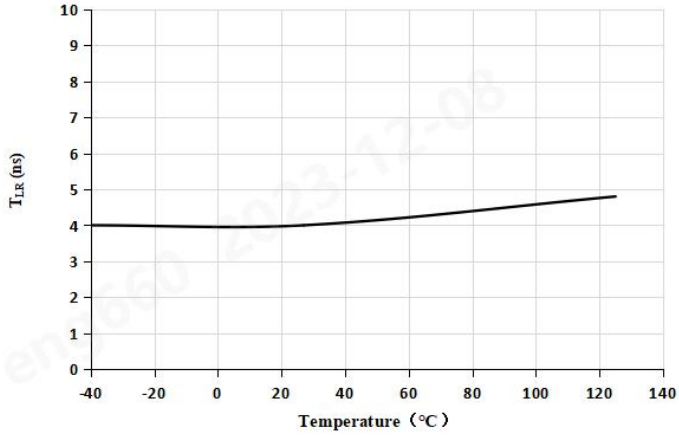


Figure 16 LO Rising Time VS Temperature

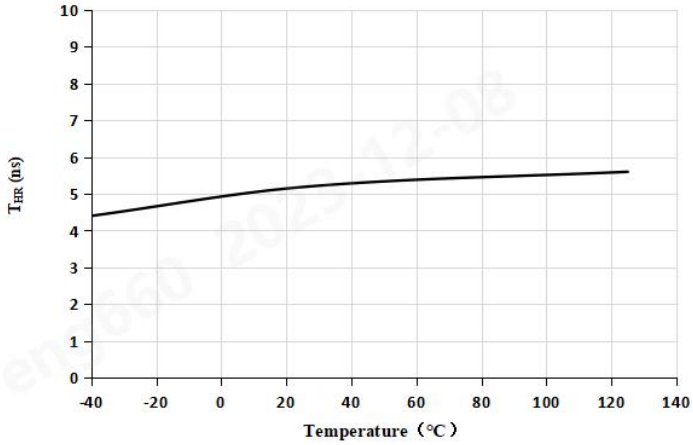


Figure 17 HO Rising Time VS Temperature

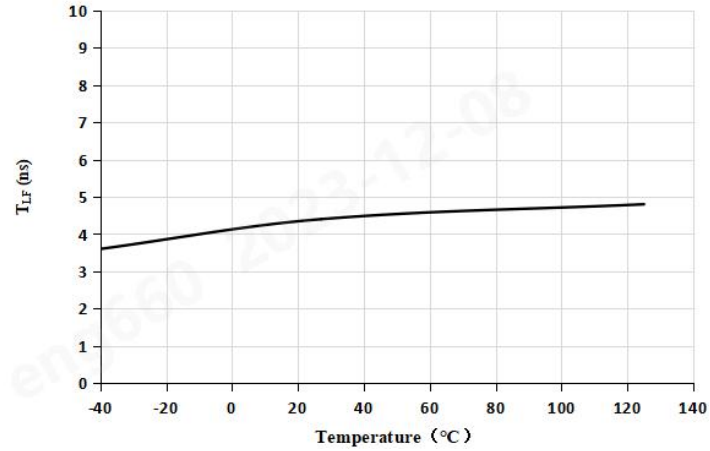


Figure 18 LO Falling Time VS Temperature

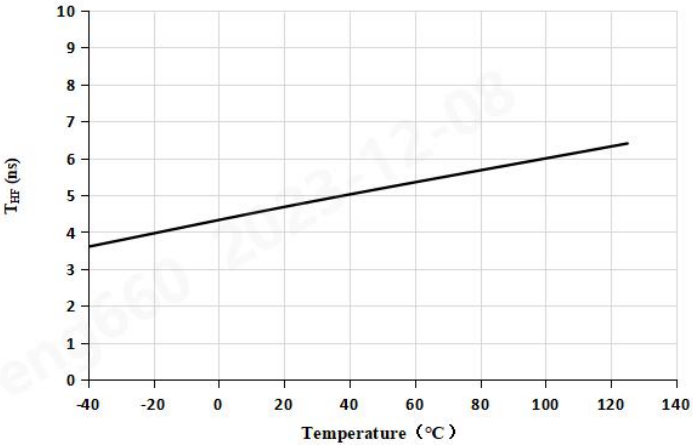


Figure 19 HO Falling Time VS Temperature

Test Waveform

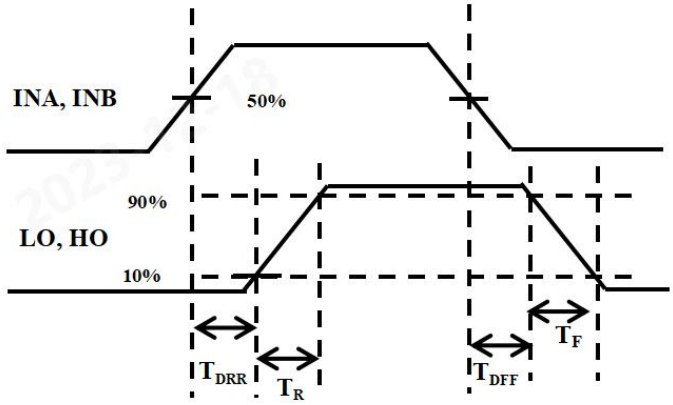


Figure 20 Waveform for Rising/Falling Edge Propagation Delay

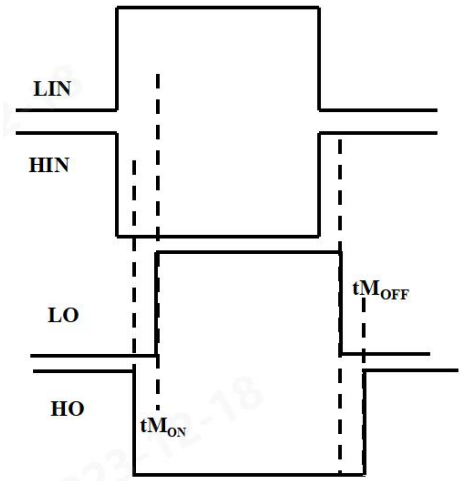


Figure 21 Waveform for Matching Delay Time

Operating Principle

SCM3510A is an integrated driver chip that integrates outputs from both high and low side drivers, providing convenience for driving half-bridge and full-bridge circuits.

This chip has built-in under voltage protection function, Under voltage lockout(UVLO) is used to prevent erroneous operation during devices startup and shutdown, as well as when the supply voltage of driver is below the specified rated operating voltage range. Both the VCC on the input side and V_B-V_{HB} on the output side have their own UVLO monitors. The input side of SCM3510A enters under voltage lockout when VCC<VCC_{OFF}. The driver outputs LO and HO remain low when input side of SCM3510A is in the under voltage lockout condition. Each driver output can independently enter under voltage lockout. For example, HO unconditionally enters under voltage lockout when V_B-V_{HB} is below V_BON, and exits under voltage lockout when V_B-V_{HB} rises above V_BON, as shown in the following figure.

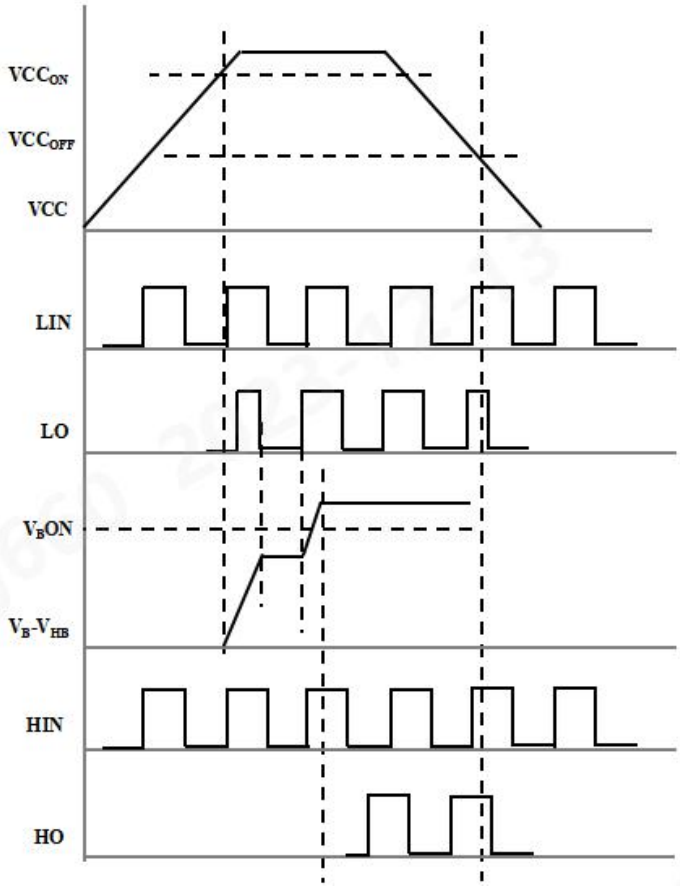


Figure 22 UVLO Sequence Diagram

Using Suggestion

1、Connect a 0.1nF, low ESR capacitor near the chip power supply port to reduce interference caused by power fluctuations on the chip(The capacitor should be as close as possible to power supply port of the chip, and it is recommended not to exceed 2mm).

2、Unused input and control ports should be pulled up or down. And pins should not be disconnected. In strong interference situation, unconnected pins can easily interfere with the operating of the chip.

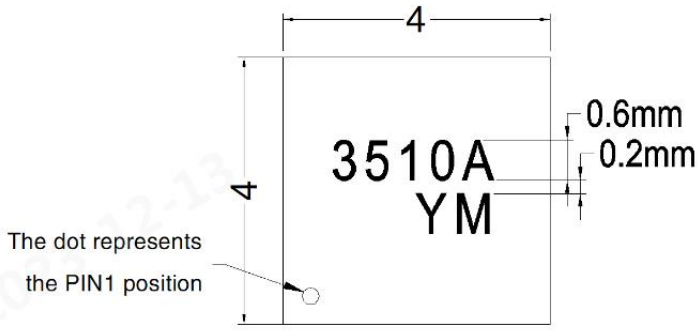
3、In order to reduce the interference caused by parasitic inductance in the output signal loop on the chip driving signal, the line from HO and LO pins to the MOSFET gate port should be as short as possible.

Ordering Information

Product Model	Package	Pin Number	Screen Printing	Packing
SCM3510AGA	LGA4x4-10L	10	3510A YM	5.7k/Plate

Product model and screen description
SCM3510XYZ:
(1)SCM3510, product code.
(2)X = A-Z, version code.
(3)Y = G, package code; G: LGA package.
(4)Z = C, I, A, M, temperature class code; C: 0℃-70℃, I: -40℃-85℃, A: -40℃-125℃, M: -55℃-125℃.
(5)YM: product trace source code; Y: product production year code, M: product production month code.

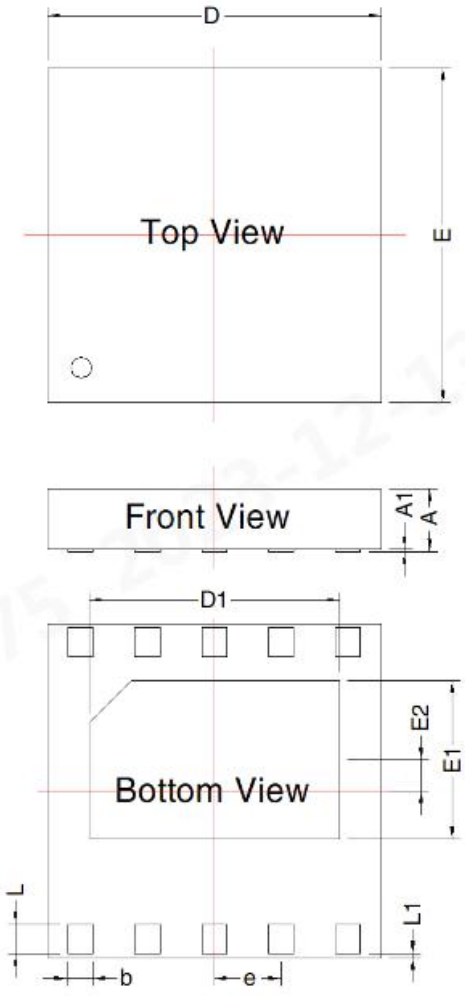
Screen Printing



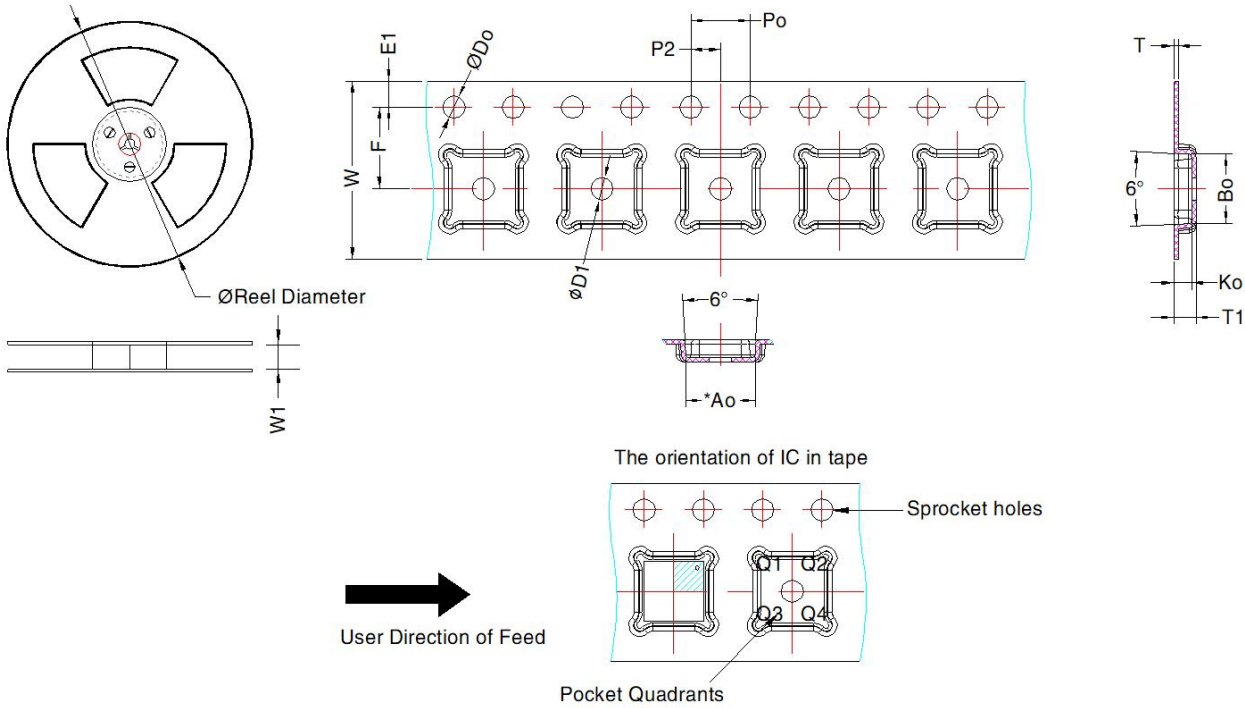
Note:
1、Typeface: Arial;
2、Character size: Height: 0.6mm, Spacing: 0.1mm, LineSpacing: 0.2mm

Package Information

THIRD ANGLE PROJECTION



LGA4x4–10L				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	0.70	0.80	0.028	0.031
A1	0	0.05	0	0.02
D	4.00 BSC		0.157 BSC	
D1	2.90	3.10	0.114	0.122
E	4.00 BSC		0.157 BSC	
E1	1.80	2.00	0.071	0.079
E2	0.37 BSC		0.015 BSC	
L	0.35	0.450	0.014	0.018
L1	0.05 BSC		0.002 BSC	
e	0.80 BSC		0.031 BSC	
b	0.25	0.35	0.010	0.014



Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E1 (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)	Pin1 Quadrant
SCM3510AGA	LGA4x4–10L	5700	330	12.4	4.47 ± 0.20	4.47 ± 0.20	1.20 ± 0.3	0.30 ± 0.05	12.0 ± 0.2	1.75 ± 0.1	5.5 ± 0.1	8.0 ± 0.3	4.0 ± 0.1	1.5 ± 0.1	1.5 ± 0.2	Q2

NOTE:
The minimum order quantity is the minimum package quantity and the order quantity must be an integer multiple of MPQ.

Mornsun Guangzhou Science & Technology Co., Ltd.

Address: No. 5, Kehui St. 1, Kehui Development Center, Science Ave., Guangzhou Science City, Luogang District, Guangzhou, P. R. China

Tel: 86-20-3860185 Fax:86-20-38601272 E-mail: info@mornsun.cn www.mornsun-power.com