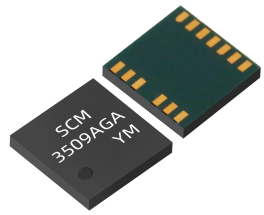
MORNSUN®

SCM3509A Dual Channel Isolated Driver

Features

- Isolated dual channel gate driver
- 2.5kV$_{RMS}$ isolated withstand voltage
- Wide input supply voltage range: 3V to 5.5V
- Drive side supply voltage: up to 25V
- Wide operation temperature: -40°C~125°C
- CMTI: ±90kV/μs
- 4A peak source current and 6A peak sink current
- 5ns maximum propagation delay matching
- 6ns maximum pulse width distortion
- Adjustable deadtime
- Low propagation delay: 25ns
- Dual channel under voltage lockout

Package



Mechanical package: LGA5x5-13L
(see "Ordering information" for details).

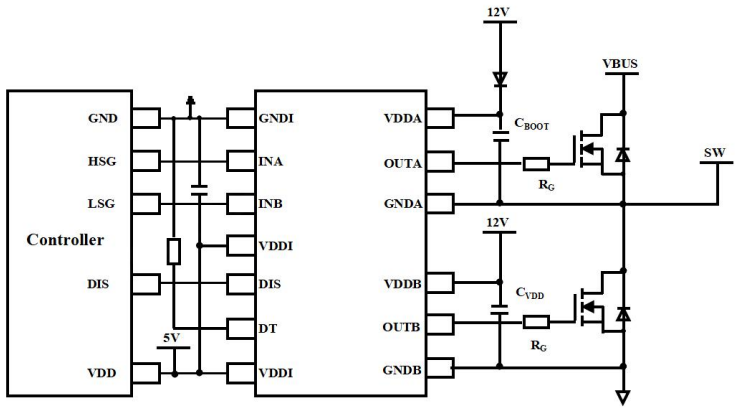
Applications

- Isolated DC-DC and AC-DC power
- DC-AC solar inverter
- Motor drive and EV charging
- UPS and battery charger
- Lighting control system

Functional Description

SCM3509A chip has excellent anti-interference ability as an isolated dual channel gate driver. Its common-mode transient immunity(CMTI) can reach 90kV/us, effectively ensuring the normal operating of the system in various harsh environments. The SCM3509A chip has a wide input power supply voltage range of 3V to 5.5V, which can provide high data transmission rate and low delay time. The LGA5x5-13L package isolation withstand voltage is up to 2.5kV$_{RMS}$ and the typical propagation delay value is 25ns with a maximum pulse width distortion of 6ns, which helps to reduce the deadtime of the power transistors and improves system efficiency. SCM3509A breaks the limitations of traditional non-isolated gate drivers through smaller package size and more powerful functional design, such as narrow operating voltage range, long propagation delay, and poor flexibility, thereby bringing higher power density and helping the system operate faster and more stable.

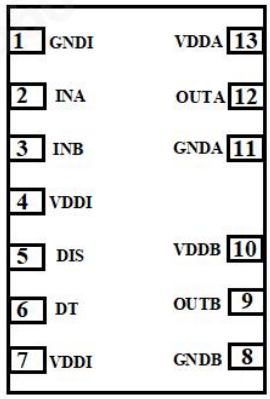
Typical Application Circuit



SCM3509A Typical Application Circuit

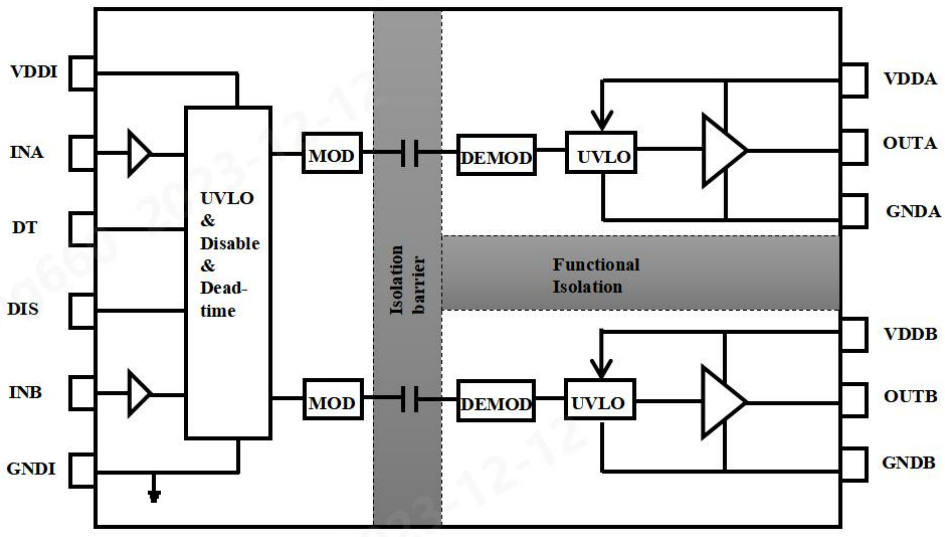
CONTENT

Pin Package



SCM3509A LGA5x5-13L Pin Package

Internal Block Diagram



SCM3509A Simplified Circuit Principles

Pin Description

Pin Name	Functional Description	
1	GNDI	Ground of input side.

2	INA	Input of driver A.
3	INB	Input of driver B.
4、7	VDDI	Input side supply voltage, It is recommended to connect to a supply of 3V to 5V.
5	DIS	Device enable. It will unconditionally drive the outputs OUTA and OUTB to low level if this input is high level. It is recommended strongly to connect this input to an external logic level to avoid errors caused by capacitor noise coupling.
6	DT	Adjustable deadtime. Connecting DT to VDDI allows the outputs to overlap. Place a 1kΩ to 200k Ω resistor (R_{DT}) between DT and GND to adjust deadtime following: t_{DT} (ns) = 10 x R_{DT} (kΩ). It is recommended to parallel a low ESR capacitor, such as 2.2nF or above.
8	GNDB	Ground of driver B.
9	OUTB	Output of driver B.
10	VDDB	Supply voltage of driver B.
11	GNDA	Ground of driver A.
12	OUTA	Output of driver A.
13	VDDA	Supply voltage of driver A.

Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (unless otherwise specified).

Symbol	Parameter Description	Min	Max	Unit
INA , INB , DIS	Voltage of the input signal to GNDI pin	-0.3	VDDI+0.3	V
	Transient voltage of the input signal to GNDI pin(50ns)	-5	VDDI+0.3	V
VDDI	Supply voltage of input side	-0.3	6	V
VDDA VDDB	Supply voltage of output side	-0.3	33	V
OUTA to GNDA OUTB to GNDB	Output voltage of driver	-0.3	VDDA+0.3 VDDB+0.3	V
	Transient output voltage of driver(200ns)	-2	VDDA+0.3 VDDB+0.3	V
-	Maximum withstand voltage (channel A to channel B) of LGA5x5-13L package	-	700	V
T_{STG}	Storage temperature	-65	150	°C
T_J	Junction temperature	-40	150	°C
ESD	HBM	-	±4000	V
	CDM	-	±1500	V

NOTE:
1. If the stress values listed in the "absolute maximum ratings" table are exceeded, it may cause permanent damage to the device. Long term operation under extreme rated conditions may affect the reliability of the devices.
2. This series of ICs includes ESD protection and is tested using the following methods: ①The ESD human body model is tested according to AEC−Q100−002 (EIA/JESD22−A114). ② The electrostatic discharge test of charged device model(CDM) is carried out in accordance with AEC−Q100−11 (EIA/JESD22−C101E).

Recommended Operating Conditions

Symbol	Parameter Description	Min	Max	Unit
VDDI	Supply voltage of input side	3	5.5	V
VDDA VDDB	Supply voltage of output side	7	25	V
INA, INB, DIS, DT	Input signal voltage	0	VDDI	V
T_J	Junction temperature	-40	150	°C
T_a	Ambient temperature	-40	125	°C

Thermal Characteristics

Symbol	Parameter Description	LGA5x5-13L	Unit
θ_{JA}	Junction-to-ambient thermal resistance[1]	209.5	°C/W
θ_{JC}	Junction-to-case thermal resistance[2]	48.4	°C/W
ψ_{JT}	Junction-to-top characteristic thermal resistance[3]	41.8	°C/W

ψ_{JB}	Junction-to-board characteristic thermal resistance[3]	31.9	°C/W

NOTE:
1.Standard JESD51-3 low effective thermal conductivity test board(1s), in an environment described in JESD51-2a.
2.Standard JESD51-3 low effective thermal conductivity test board(1s), by transient dual interface test method described in JESD51-14.
3.Obtained by simulating in an environment described in JESD51-2a.

Electrical Characteristics

General test conditions: Free-air, normal operating temperature range. No load(unless otherwise specified).

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Input Characteristics						
R_{INA_PD} R_{INB_PD}	Input Pull Down Resistance	-	-	100	-	kΩ
R_{DIS_PD}	DIS Pin Pull Down Resistance	-	-	100	-	kΩ
$VDDI_H$	Input Supply UVLO Rising Threshold	-	2.35	2.55	2.75	V
$VDDI_L$	Input Supply UVLO Falling Threshold	-	2.15	2.35	2.55	V
V_{VDDI_HYS}	Input Supply UVLO Hysteresis	-	-	0.2	-	V
V_{VIA_H} V_{VIB_H}	Logic High Input Threshold	-	-	1.6	2	V
V_{VIA_L} V_{VIB_L}	Logic Low Input Threshold	-	0.8	1.2	-	V
V_{INA_HYS} V_{INB_HYS}	Input Hysteresis	-	-	0.4	-	V
I_{VDDIQ}	Input Supply Quiescent Current	INA=0, INB=0	-	0.75	2	mA
I_{VDDI}	Input Supply Operating Current	Input frequency =500kHz, $C_{OUTA/B}$=0	-	1.8	-	mA
Output Characteristics						
V_{VDDA} V_{VDDB}	Output Side Supply Voltage	Minimum defined by UVLO	-	-	25	V
I_{VDDAQ} I_{VDDBQ}	Output Supply Quiescent Current	INA=0, INB=0		0.9		mA
I_{VDDA} I_{VDDB}	Output Supply Operation Current	Input frequency=500kHz	-	2.75	3.35	mA
V_{OUTA_L} V_{OUTB_L}	Logic Low Output Voltage	I_{OUT}=-100mA	-	0.06	-	V
V_{VDDA} -V_{OUTA_H} V_{VDDB} -V_{OUTB_H}	Logic High Output Voltage	I_{OUT}=100mA	-	0.12	-	V
R_{OUTA_L} R_{OUTB_L}	Logic Low Output Resistance	I_{OUT}=-100mA	-	0.6	-	Ω
R_{OUTA_H} R_{OUTB_H}	Logic High Output Resistance	I_{OUT}=100mA	-	1.2	-	Ω
I_{OUTA+} I_{OUTB+}	Output Source Current	V_{OUT}=0V	-	4	-	A
I_{OUTA-} I_{OUTB-}	Output Sink Current	V_{OUT}=12V	-	6	-	A

SCM3509A(LGA5x5-13L)

Under Voltage Lockout Characteristics						
$VDDA_H$ $VDDB_H$	Output Supply UVLO Rising Threshold	-	5.6	6.25	6.9	V
$VDDA_L$ $VDDB_L$	Output Supply UVLO Falling Threshold	-	5.1	5.75	6.4	V
V_{VDDA_HYS} V_{VDDB_HYS}	Output Supply UVLO Hysteresis	-	-	0.5	-	V

Switching Characteristics

VDDI = 3.3 /5 V, VDDA = VDDB = 12 V. Ta= - 40 °C to125 °C .

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
t_{PWmin}	Minimum Pulse Width	$C_{OUTA/B}$=0	-	-	35	ns
T_{PWD}	Pulse Width Distortion |t_{PDLH} - t_{PDHL}|	-	-	-	6	ns
t_{PDHL} t_{PDLH}	Propagation Delay	-	10	25	35	ns
t_{DMHL} t_{DMLH}	Channel to Channel Delay Matching	-	-	-	5	ns
t_{DT}	Deadtime [1]	t_{DT} (ns)=10*R(kΩ), R=20kΩ	160	200	240	ns

t_R	Output Rise Time(10% to 90%)	$C_{OUTA/B}$=1nF	-	8	15	ns
t_F	Output Fall Time(90% to 10%)	$C_{OUTA/B}$=1nF	-	8	15	ns
t_{DIS}	Disable-Shutdown Time	-	-	-	40	ns
t_{EN}	Disable Recovery Time	-	-	-	55	ns
t_{start_VDDI}	VDDI Power-up Delay Time	Time from VDDI = VDDI_ON to OUTA/B = INA/B(INA or INB Connect to VDDI)	-	8.5	15	μs
t_{start_VDDA} t_{start_VDDB}	VDDA/B Power-up Delay Time	(Time from VDDA/B = 2V to OUTA/B = INA/B(INA or INB Connect to VDDI, $C_{OUTA/B}$=1nF)	-	18	30	μs
CMTI	Common Mode Transient Immunity	-	-	±90	-	kV/μs

NOTE:
1. The deadtime is adjustable, see the DT pin description for details.

Isolation Characteristics

Symbol	Parameter	Test Condition	Value	Unit
Conventional Isolation Parameter				
CLR	Min. External Air Gap	Measure the shortest external air distance between input and output	3.5	mm
CPG	Min. External Tracking	Measure the shortest external housing distance between input and output	3.5	mm
DTI	Distance Through the Insulation	Minimum internal gap(internal distance)	32	μm
CTI	Comparative Tracking Index	DIN DIS 60112(VDE 0303-11); IEC60112	>600	V
	Material Group	IEC 60112	I	-
DIN VDE 0110				
	For Rated Mains Voltage≤150V_{RMS}	-	I-III	-
	For Rated Mains Voltage≤300V_{RMS}	-	I-III	-
	For Rated Mains Voltage≤600V_{RMS}	-	I	-
	For Rated Mains Voltage≤1000V_{RMS}	-	/	-
DIN V VDE V 0884-11 : 2017-01				
V_{IORM}	Maximum Repetitive Isolation Voltage	-	792	V_{PK}
V_{IOWM}	Maximum Operating Isolation Voltage	AC voltage; TDDB test	560	V_{RMS}
		DC voltage	792	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST}=V_{IOTM} t=60s(certification) V_{TEST}=1.2×V_{IOTM} t=1s(100% production test)	3535	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	Test method according to IEC62368-1, 1.2/50μs Waveform, V_{TEST}=1.6×V_{IOSM}	/	V_{PK}
		Test method according to IEC62368-1, 1.2/50μs Waveform, V_{TEST}=1.3×V_{IOSM}	3500	V_{PK}
$V_{pd(m)}$	Input to Output Test Voltage, Method B1	$V_{ini.b}$ = V_{IOTM}, $V_{pd(m)}$ = V_{IORM} × 1.5, t_{ini} = t_m = 1 sec, q_{pd} ≤ 5 pC (100% production test)	1188	V_{PK}
$V_{pd(m)}$		$V_{ini.b}$ = V_{IOTM}, $V_{pd(m)}$ = V_{IORM} × 1.875, t_{ini} = t_m =1 sec, q_{pd} ≤ 5 pC (100% production test)	/	V_{PK}
$V_{pd(m)}$	Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{ini.b}$ = V_{IOTM}, $V_{pd(m)}$ = V_{IORM} × 1.3, t_{ini} = 60 sec, t_m = 10 sec, q_{pd} ≤ 5 pC	1030	V_{PK}
$V_{pd(m)}$		$V_{ini.b}$ = V_{IOTM}, $V_{pd(m)}$ = V_{IORM} × 1.6, t_{ini} = 60 sec, t m = 10 sec, q_{pd} ≤ 5 pC	/	V_{PK}
$V_{pd(m)}$	Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{ini.a}$ = V_{IOTM}, $V_{pd(m)}$ = V_{IORM} × 1.2, t_{ini} = 60 sec, t_m = 10 sec, q_{pd} ≤ 5 pC	950	V_{PK}

C_{IO}	Isolation Capacitance, Input to Output	V_{IO}=0.4×sin(2πft), f=1MHz, VDDI=5V	1.2	pF
R_{IO}	Isolation Resistance	V_{IO}=500V, T_{amb}=T_s	>10^9	Ω
		V_{IO}=500V, 100℃≤T_{amb}≤125℃	>10^{11}	Ω
	Climatic Category	-	40/125/21	
	Pollution Degree	DIN VDE 0110 table1	2	-
UL1577				
V_{ISON}	Maximum Isolation Voltage	V_{TEST}=1.2×V_{ISON}, t=1s(100% production test)	2.5	kV_{RMS}

NOTE:
1. The isolation characteristics is being certificated. The data will be updated after the certification is complete.

Safety limit value

LGA5x5-13L basic safety limit values according to VDE-0884-11

Description	Test Condition	Parameter	Value	Unit
Input Power	$R_{\theta JA}$=209.5°C/W [1], T_J=150°C, T_A=25°C	VDDI Input	12	mW
		INA, INB	293	mW
		All Input	598	mW
Safety Current	$R_{\theta JA}$=209.5°C/ W [1] , VDDA/B=12V, T_J =150°C, T_A=25°C	INA, INB	24.4	mA
	$R_{\theta JA}$=209.5°C/ W [1] , VDDA/B=25V, T_J =150°C, T_A=25°C	INA, INB	11.7	mA
Safety Temperature[2]	-	-	150	℃

NOTE:
1. Calculate with the junction-to-air thermal resistance, which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2. The maximum safety temperature has the same value as the maximum junction temperature.
3. Safety limit value is being certificated. The data will be updated after the certification is complete.

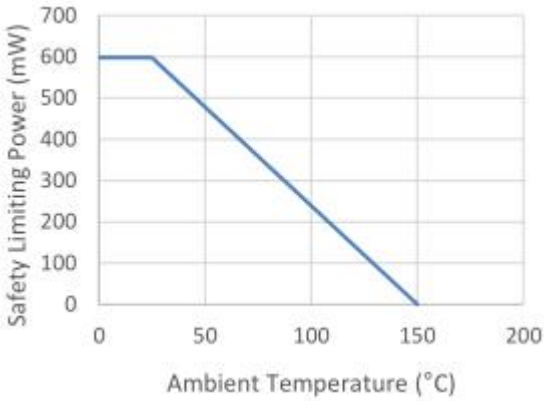


Figure 1 Input Power VS Temperature

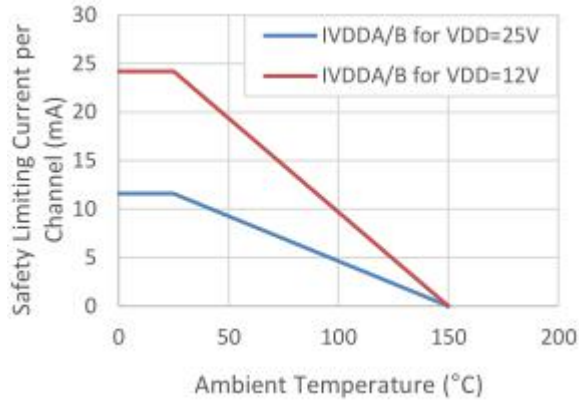


Figure 2 Supply Current VS Temperature

Certification information

SCM3509A(LGA5x5-13L)certification information table

Certification Authority	Certification Standard	Test Condition
CSA	Approved under CSA Component Acceptance Notice 5A	Single protection, 2500Vrms isolation voltage
VDE	DIN VDE V 0884-11: 2017-01	basic insulation operating voltage V_{IORM}=792V_{PEAK} basic insulation operating voltage V_{IOSM}=3500V_{PEAK} basic insulation operating voltage V_{IOTM}=3535V_{PEAK}
UL	UL1577	Single protection, 2500Vrms isolation voltage
CQC	Certified by CQC11-471543-2012	basic insulation.
	GB4943.1-2011	

NOTE:
1. The certification information is being certificated. The data will be updated after the certification is complete.

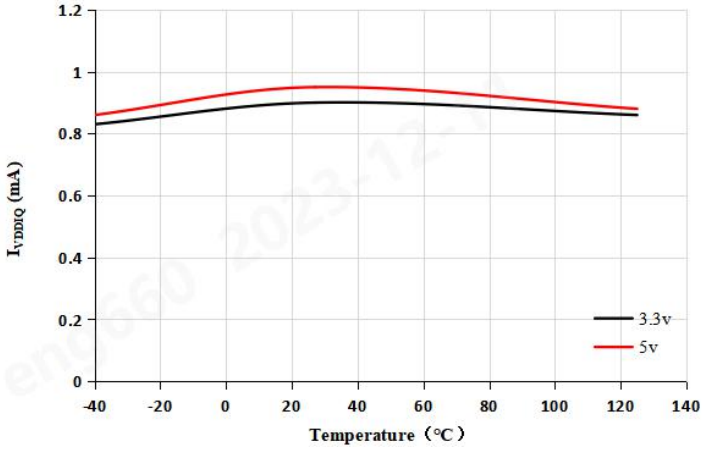


Figure 3 VDDI Quiescent Current VS Temperature

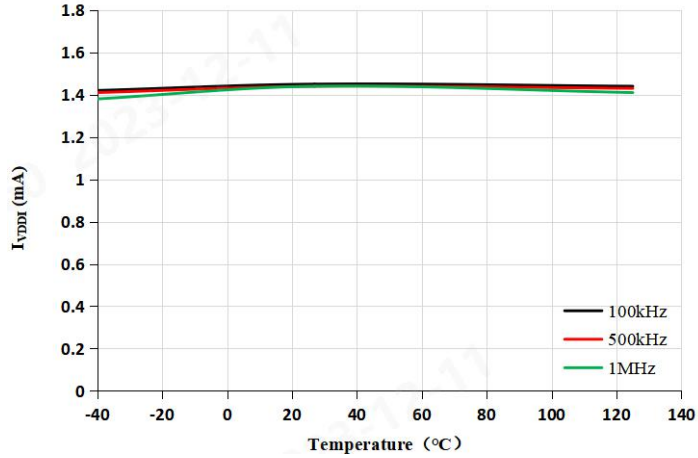


Figure 4 VDDI Operating Current VS Temperature

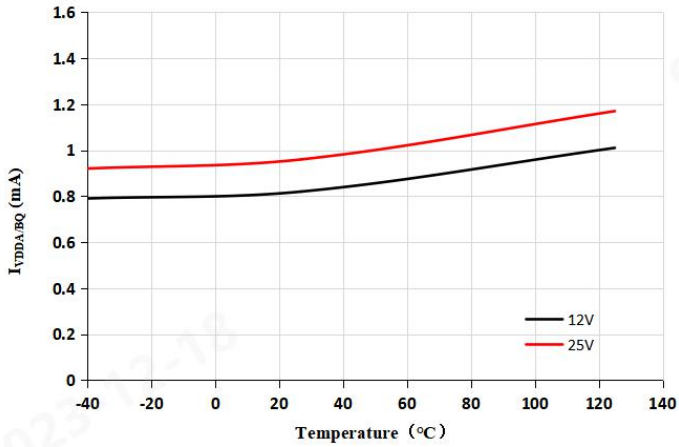


Figure 5 VDDA/B Quiescent Current VS Temperature

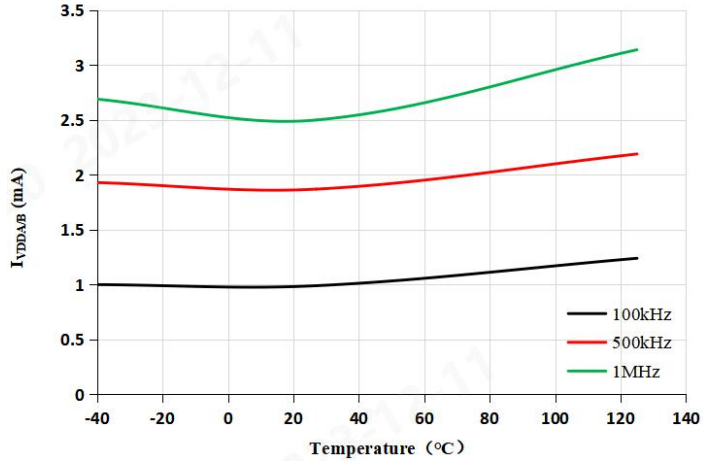


Figure 6 VDDA/B Operating Current VS Temperature

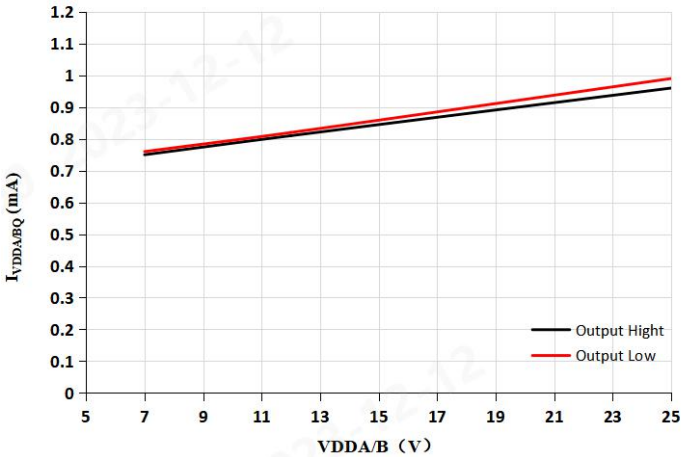


Figure 7 VDDA/B Quiescent Current VS Supply Voltage

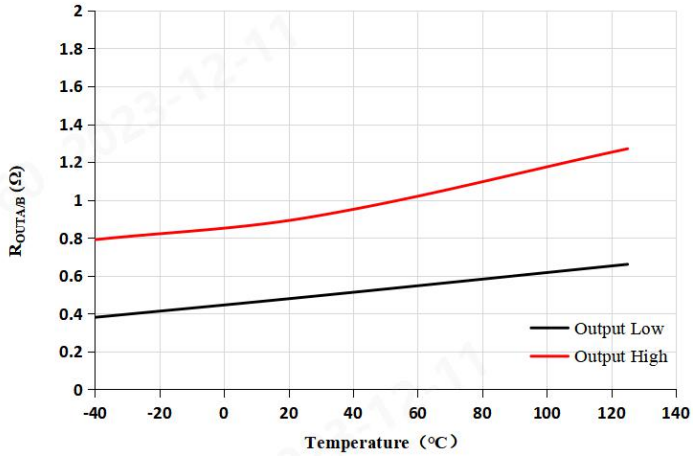


Figure 8 Output Resistance VS Temperature

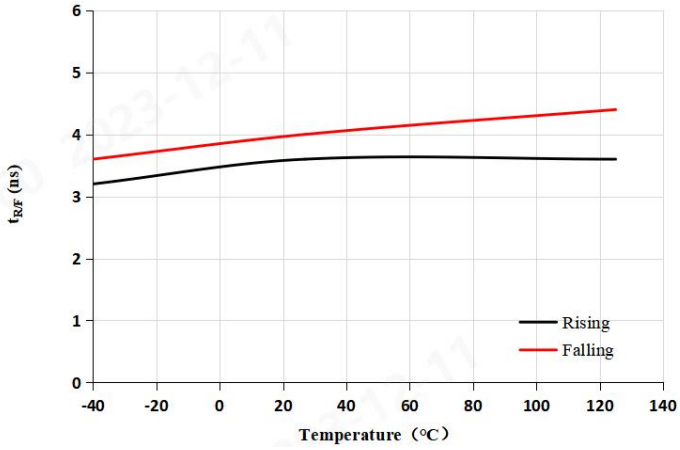


Figure 9 Typical Rising/Falling Time VS Temperature

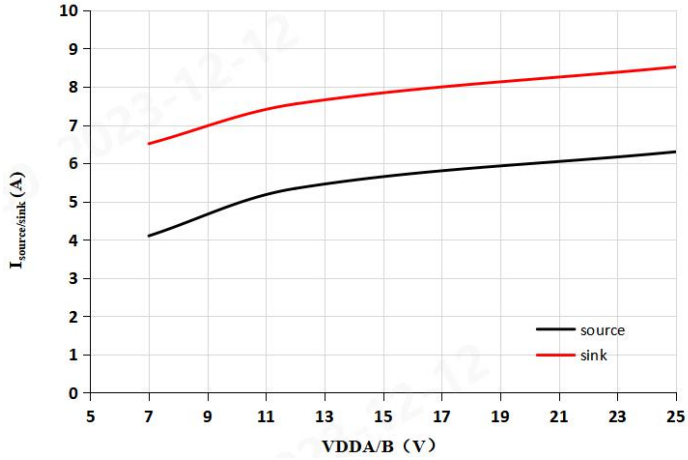


Figure 10 Output Source/Sink Current VS VDDA/B Supply Voltage

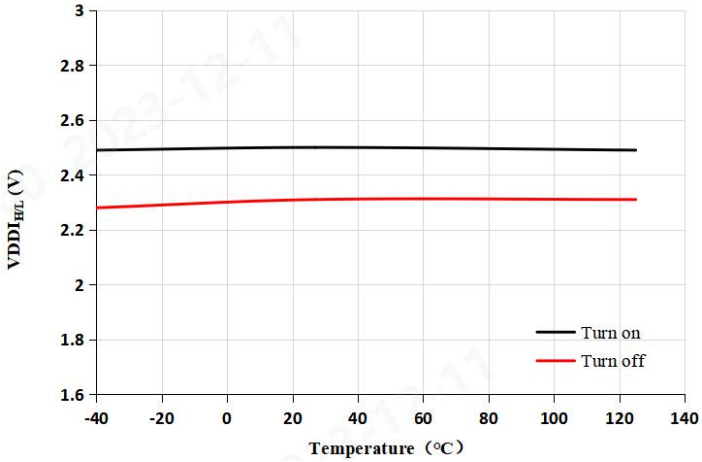


Figure 11 VDDI UVLO VS Temperature

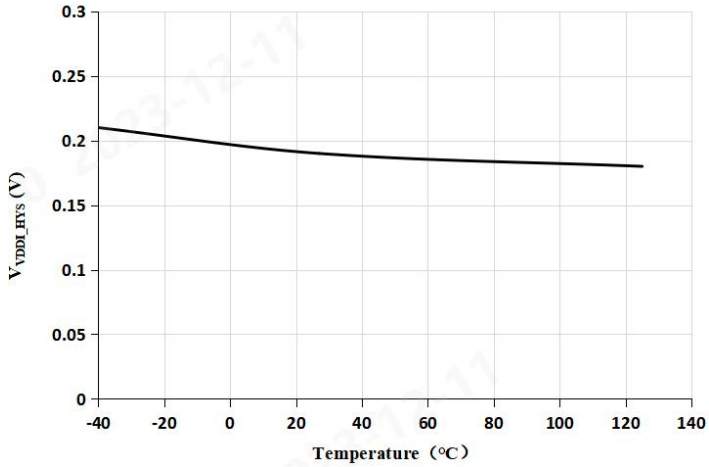


Figure 12 VDDI UVLO Hysteresis VS Temperature

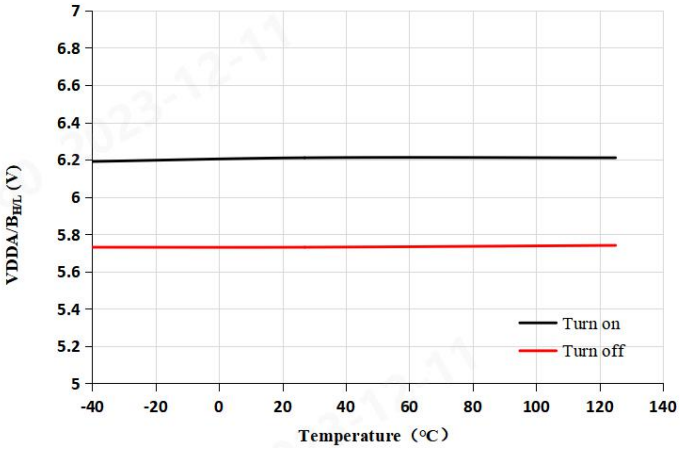


Figure 13 VDDA/B UVLO VS Temperature

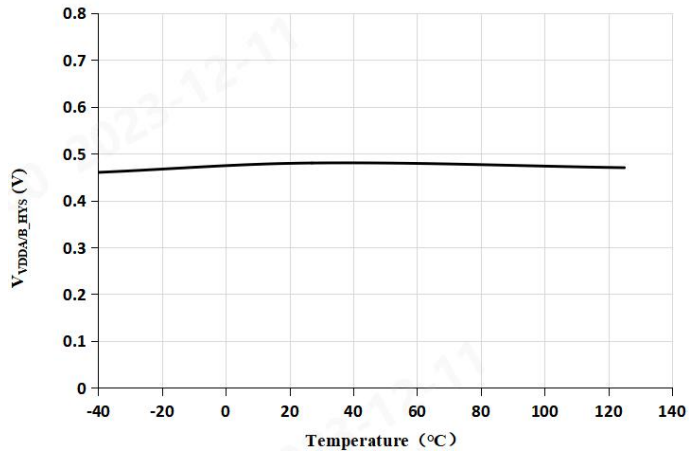


Figure 14 VDDA/B UVLO Hysteresis VS Temperature

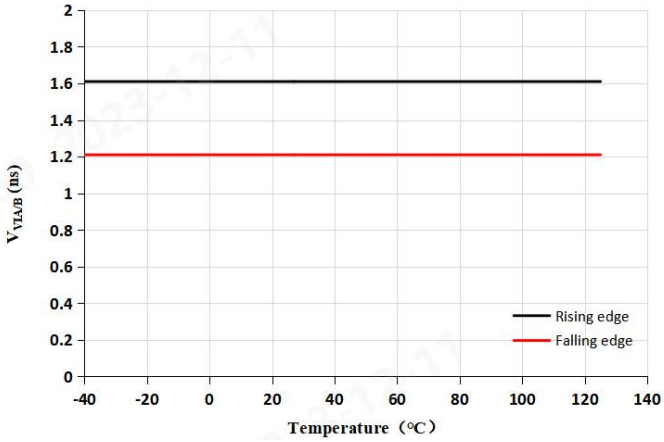


Figure 15 INA /INB UVLO VS Temperature

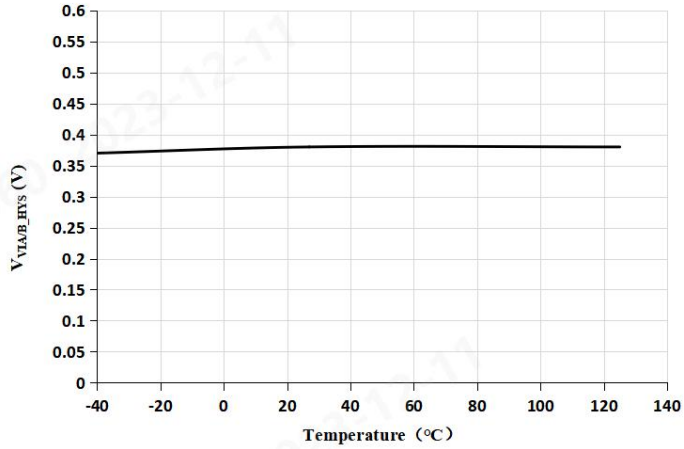


Figure 16 INA /INB UVLO Hysteresis VS Temperature

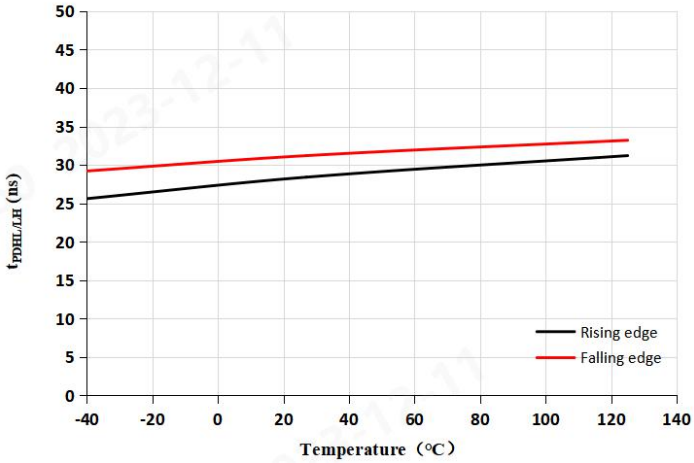


Figure 17 Propagation Delay VS Temperature

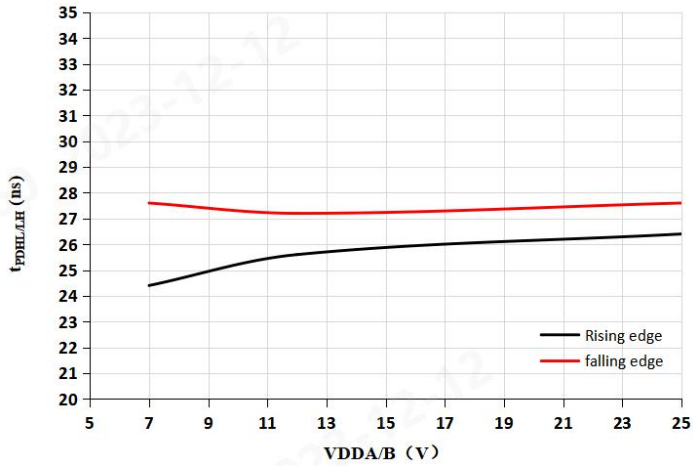


Figure 18 Propagation Delay VS VDDA/B

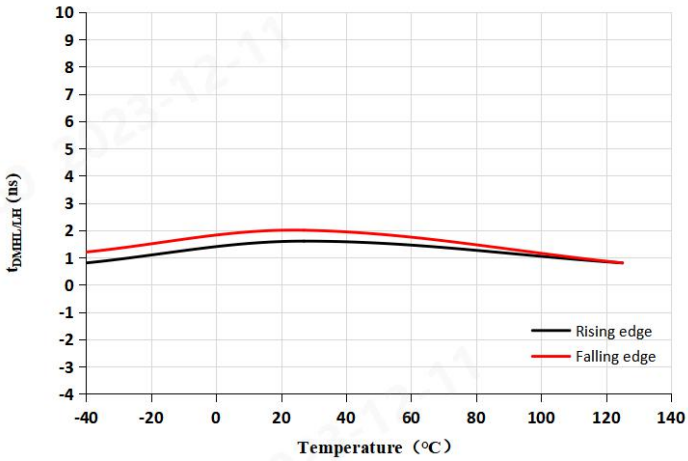


Figure 19 Propagation Matching Delay VS Temperature

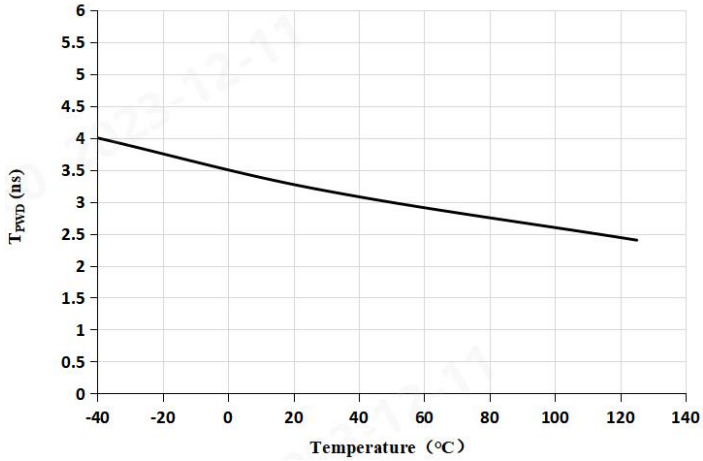


Figure 20 Pulse Width Distortion VS Temperature

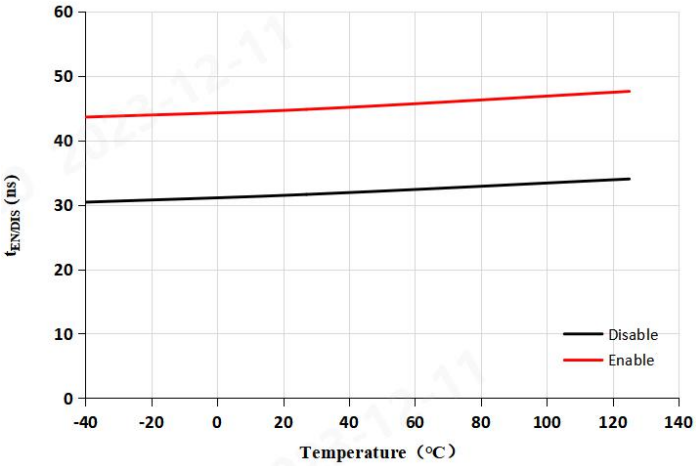


Figure 21 Enable/Disable VS Temperature

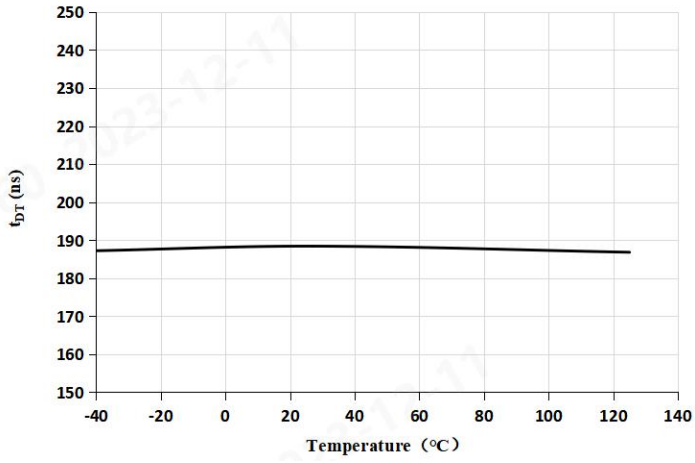


Figure 22 Deadtime(R_{DT}=20kΩ) VS Temperature

Test Circuit

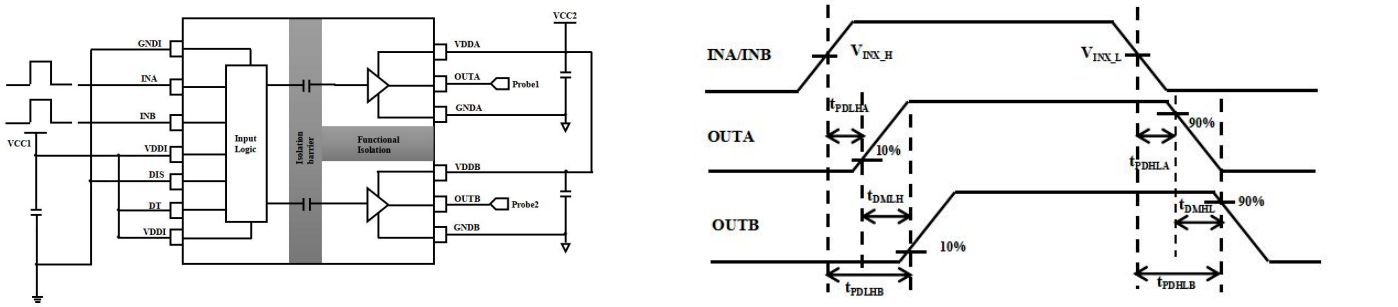


Figure 23 Test Circuit and Waveform for Rising/Falling Edge Propagation Delay

NOTE: DT pin connects to VDDI.

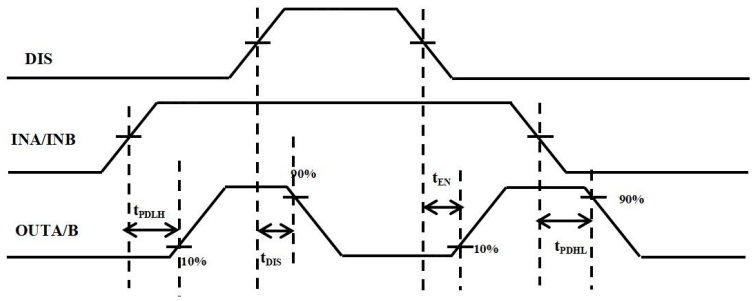


Figure 24 Test Waveform for Enable/Disable Propagation Delay Time

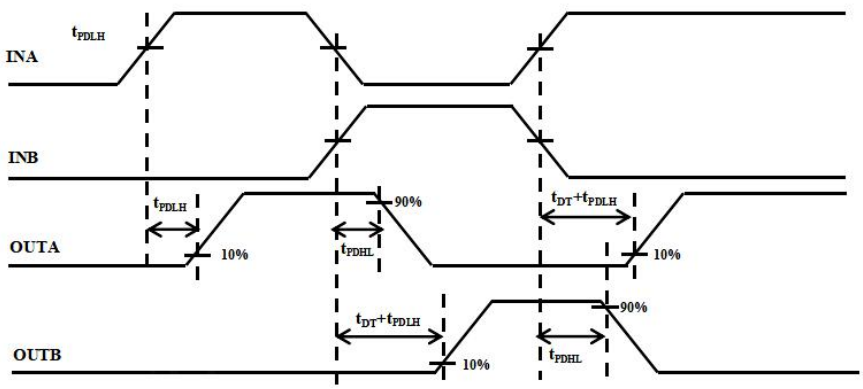


Figure 25 Test Waveform for Deadtime

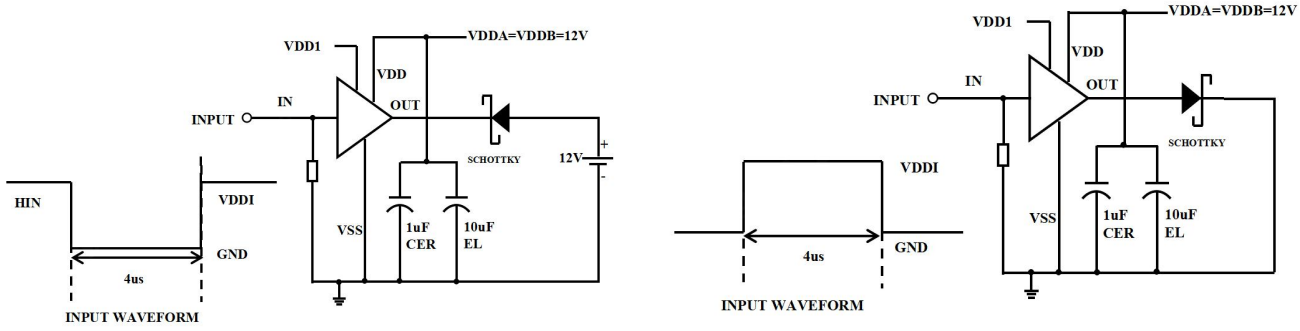


Figure 26 Test Circuit for the Ability of Source/Sink Current

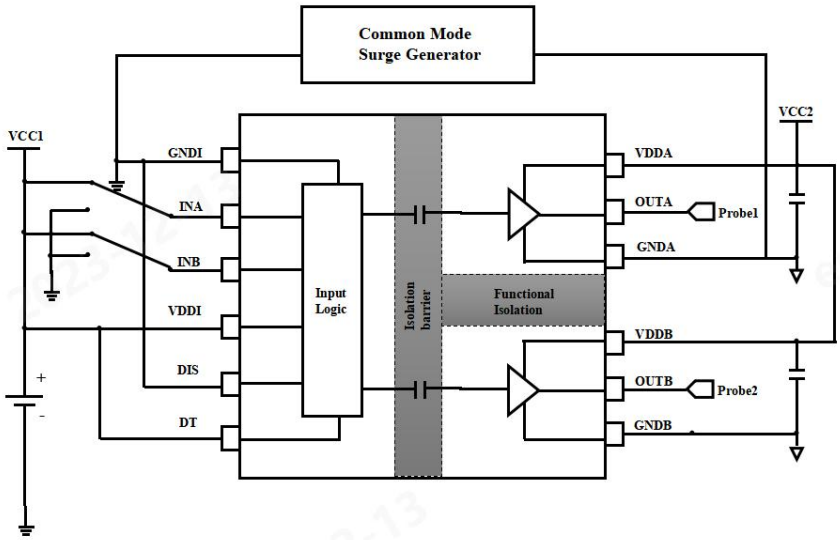


Figure 27 Test Circuit for CMTI

Operating Principle

SCM3509A is a dual channel isolated driver IC which supports two independent and isolated driver output. This chip also has built-in under voltage protection and over voltage protection functions.

Disable function: The chip defaults to outputting high or low level, when the input is suspended. After the DIS input becomes high, the OUTA and OUTB will unconditionally become low, regardless of the states of INA and INB. After DIS=VIH, devices will stop operating within t_{SD} and recover within $t_{RESTART}$ after DIS=VIL. If VDDI is below its UVLO voltage(OUTA/OUTB is still low), the DIS input is invalid.

Under voltage lockout: under voltage lockout(UVLO) is used to prevent erroneous operation during devices startup and shutdown, as well as when the supply voltage of driver is below the specified rated operating voltage range. Both driver A and driver B on the input side have their own UVLO monitors. SCM3509A enters under voltage lockout on the input side when VDDI<$VDDI_L$, and exits under voltage lockout when VDDI>$VDDI_H$. The OUTA and OUTB remain at a low level when the input side of SCM3509A is in the under voltage lockout condition, and their own supply voltage(VDDA, VDDB) are within the tolerance range. Each driver output can independently enter under voltage lockout. For example, OUTA unconditionally enters under voltage lockout when VDDA is below $VDDA_L$ and exits under voltage lockout when VDDA rises above $VDDA_H$.

3. Simultaneous conduction protection: The deadtime of OUTA and OUTB can be adjusted by configuring the resistance R_{DT} between DT pin and GND pin. The calculation formula is t_{DT}(ns)≈10*R_{DT}(kΩ). The recommended resistance range for RDT is (1kΩ≤R_{DT}≤200kΩ). When R_{DT}=100kΩ, the voltage of the DT pin under steady state voltage is about 0.8V, and the current on R_{DT} does not exceed 10μA. If the DT pin is suspended, the deadtime is set to no more than 35ns by default.

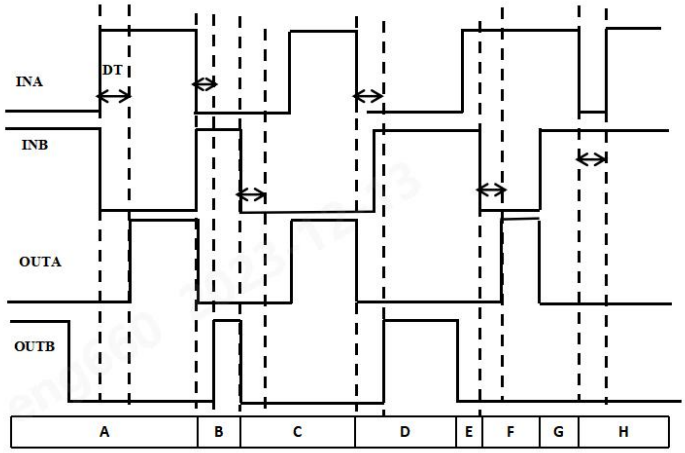


Figure 28 The Waveform of Simultaneous Conduction Protection

Number	Input Condition	Output Condition
A	INA goes high, and INB goes low.	OUTB goes low immediately, then OUTA goes high after the programmed deadtime which is assigned at INB goes low.
B	INA goes low, and INB goes high.	OUTA goes low immediately, then OUTB goes high after the programmed deadtime which is assigned at INA goes low.
C	INB goes low, then INA goes high after deadtime.	OUTB goes low immediately, then OUTA goes high immediately when INA goes high.
D	INA goes low, then INB goes high before deadtime.	OUTA goes low immediately, then OUTB goes high after deadtime
E	INA goes high, INB is still high	OUTB goes low immediately and OUTA keeps low.
F	INA is still high, INB goes low.	OUTA goes high after deadtime while INB is low and OUTB keeps low.
G	INA is still high, INB goes high after deadtime	OUTA goes low immediately and OUTB keeps low.
H	INA goes low then goes high before deadtime while INB is still high.	OUTA keeps low and OUTB keeps low because deadtime control.

Truth Table

Number	DIS	VDDI	VDDA/B	Input		Output		Note
				INA	INB	OUTA	OUTB	
1	L or O	PU	PU	L	H	L	H	If deadtime function is used, output goes high after the deadtime finishes.
2	L or O	PU	PU	H	L	H	L	
3	L or O	PU	PU	H	H	H	H	DT pin is connected to VDDI.
4	L or O	PU	PU	H	H	L	L	DT pin is suspended or connected with R_{DT}.
5	L or O	PU	PU	L	L	L	L	
6	L or O	PU	PU	O	O	L	L	
7	H	PU	PU	X	X	L	L	
8	X	PU	PD	X	X	L	L	
9	X	PD	PU	X	X	L	L	

NOTE:

1、PD=power down, PU=power up, H=logic high level, L=logic low level, O=floating, X=any state.

Using Suggestion

1、Isolation requires compulsively separate power supply for VDDI, VDDA and VDDB. Connect a 0.1nF, low ESR capacitor near the chip power supply port to reduce interference caused by power fluctuations on the chip(The capacitor should be as close as possible to power supply port of the chip, and it is recommended not to exceed 2mm).

2、Unused input and control ports should be pulled up or down. And pins should not be disconnected. In strong interference situation, unconnected pins can easily interfere with the operating of the chip.

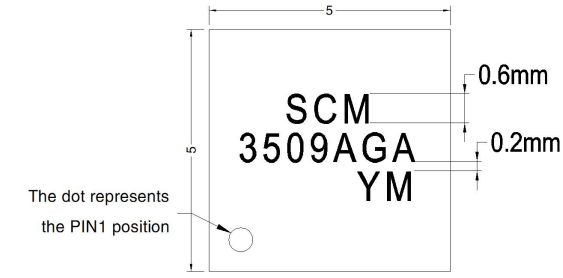
Ordering Information

Product Model	Package	Pin Number	Screen Printing	Packing
SCM3509AGA	LGA5x5-13L	13	SCM 3509AGA YM	5.4k/Plate

Product model and screen description
SCM3509XYZ:
(1)SCM3509, product code.

(2)X = A-Z, version code.
(3)Y = G package code; G: LGA package.
(4)Z = C, I, A, M, temperature class code; C: 0℃-70℃, I: -40℃-85℃, A: -40℃-125℃, M: -55℃-125℃.
(5)YM: product trace source code; Y: product production year code, M: product production month code.

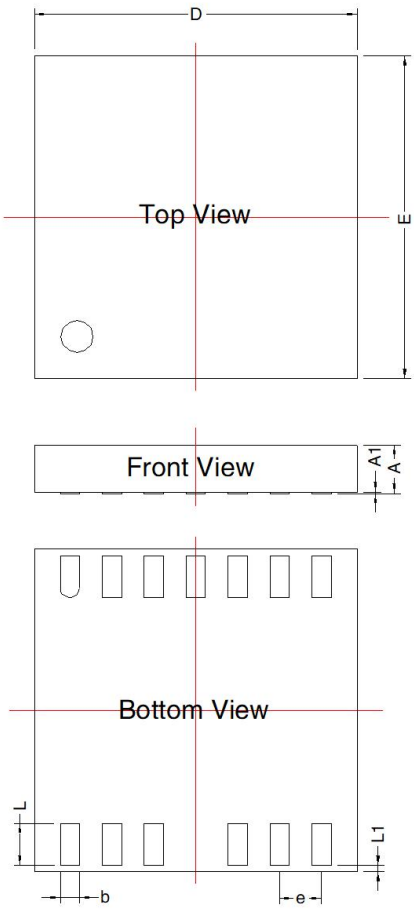
Screen Printing



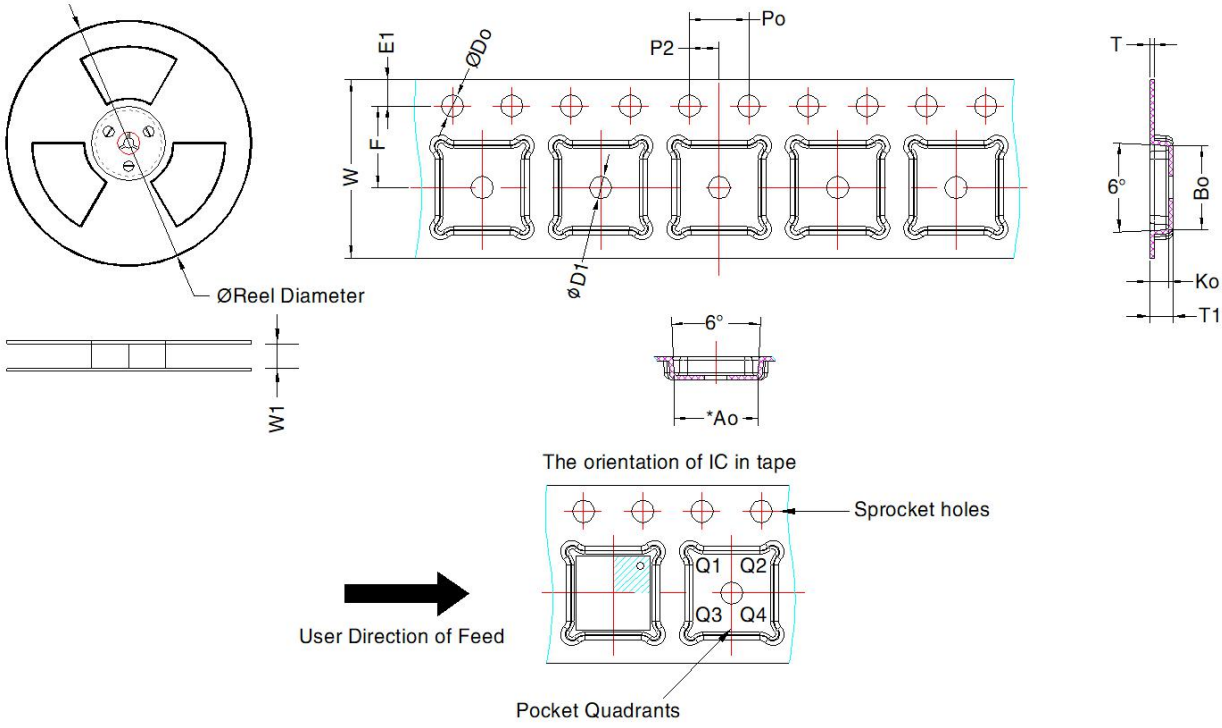
Note:
1、Typeface: Arial;
2、Character size: Height: 0.6mm, Spacing: 0.1mm, LineSpacing: 0.2mm

Package Information

THIRD ANGLE PROJECTION



LGA5x5-13L				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	0.70	0.80	0.028	0.031
A1	0	0.05	0	0.002
D	5.00 BSC.		0.197 BSC.	
E	5.00 BSC.		0.197 BSC.	
L	0.60	0.70	0.024	0.28
L1	0.10 BSC		0.004 BSC	
e	0.65 BSC		0.026 BSC	
b	0.250	0.350	0.010	0.014



Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E1 (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)	Pin1 Quadrant
SCM3509AGA	LGA5x5–13L	5400	330	12.4	5.48 ± 0.20	5.48 ± 0.20	1.30 ± 0.3	0.30 ± 0.05	12.0 ± 0.2	1.75 ± 0.1	5.5 ± 0.1	8.0 ± 0.3	4.0 ± 0.1	1.5 ± 0.1	1.5 ± 0.2	Q2

NOTE:
The minimum order quantity is the minimum package quantity and the order quantity must be an integer multiple of MPQ.

Mornsun Guangzhou Science & Technology Co., Ltd.

Address: No. 5, Kehui St. 1, Kehui Development Center, Science Ave., Guangzhou Science City, Luogang District, Guangzhou, P. R. China

Tel: 86-20-3860185 Fax:86-20-38601272 E-mail: info@mornsun.cn www.mornsun-power.com