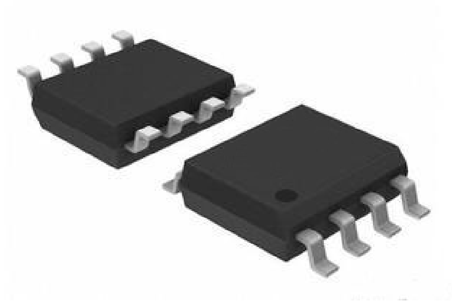
SCM3504C High Side Gate Driver

FEATURES

- High voltage range: Up to 700 V
- Simple circuit architecture and low power consumption
- High dv/dt Immunity
- 3 A Source / 3 A Sink Currents
- Typical 60 ns Propagation Delay
- The VDD undervoltage locking

PACKAGE



Product package: SOT8.

Please see “Ordering Information” for details

APPLICATIONS

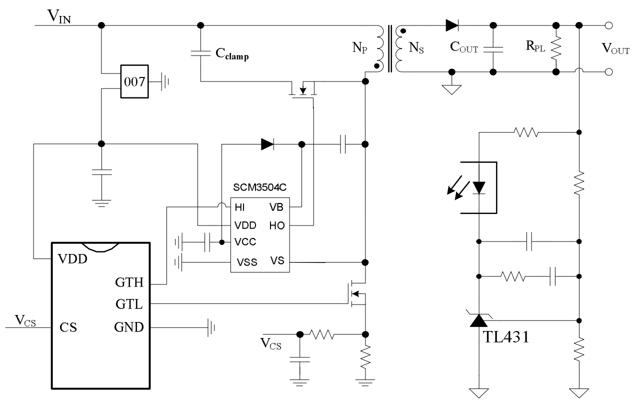
- Engine Drive
- Electron Ballast

FUNCTIONS

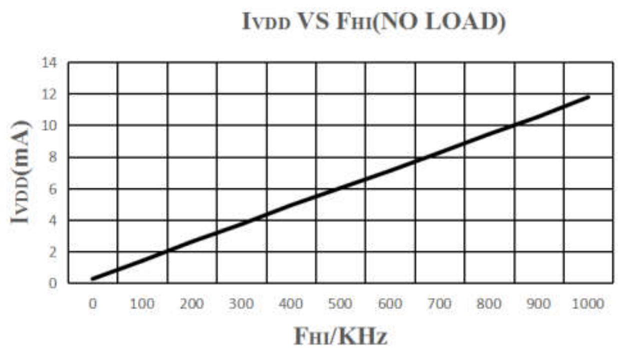
SCM3504C is a high side gate driver that can drive the high side MOSFET or IGBT in a voltage range of 0 to 700 V.

SCM3504C has full difference level shift circuit, which can operate reliably in the noise environment of ultra-high dv/dt; the typical value of source/sink current is 3A/3A, which can realize high frequency and high power gate drive.

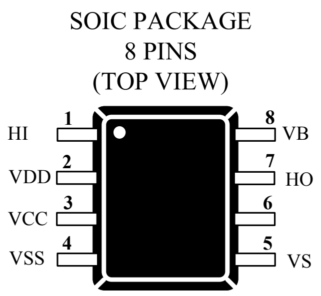
TYPICAL APPLICATION CIRCUIT



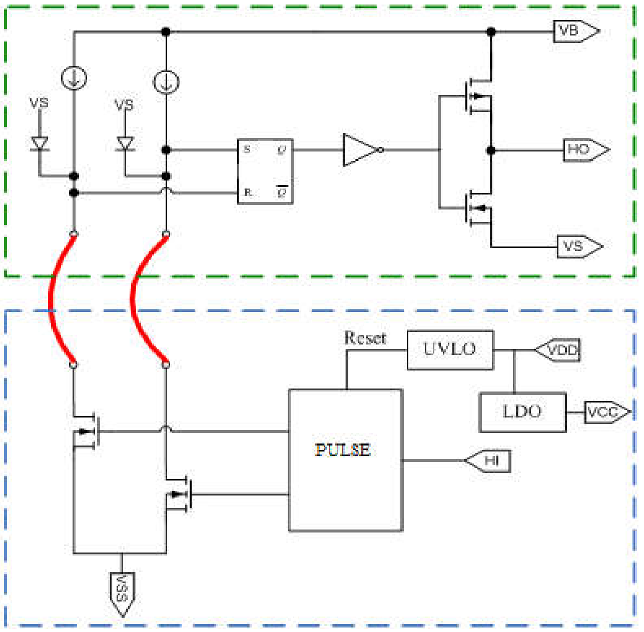
FUNCTIONAL CURVE



PINOUT INFORMATION



INTERNAL BLOCK DIAGRAM



PIN DESCRITION

Pin Out	Name	I/O	Function
1	HI	I	High side input
2	VDD	P	An external bypass capacitance is required to power the chip, Low side supply voltage
3	VCC	P	The low side chip LDO output, which charges the bootstrapped capacitor through the high voltage diode, requires external capacitance to the VSS
4	VSS	P	Ground reference
5	VS	P	High side supply return
6			
7	HO	O	High side output
8	VB	P	High side supply

ABSOLUTE MAXIMUM RATINGS

The following data are measured within the natural ventilation, normal operating temperature range (unless otherwise stated).

Symbol	Parameters	Min	Max	Unit
V_{VB}-V_{VS}	High side floating voltage	-0.3	15	V
V_{VB}	High side boot pin voltage	-1	715	
V_{VS}	High side supply return reference ground voltage	-1	700	
V_{HO}	High side drive output voltage	V_{VS}-0.7	V_{VB}+0.7	
V_{VDD}	Low side supply voltage	-0.3	30	
V_{VCC}	The VCC pin voltage	11.5	13.5	V
V_{HI}	Drive input voltage	-0.3	V_{VDD}+0.3	V
T_J	Operating junction temperature range	-40	125	℃
T_{STG}	Storage temperature	-55	150	
	Within 10 seconds, Binding wire temperature at a distance of 0.6mm from the shell.		260	
	ESD (HUMAN BODY MODE)	±4000		V

REMARKS: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. All voltage values are based on the earth (GND) as a reference. The current is a positive input and a negative output of the specified terminal.

ELECTRICAL CHARACTERISTICS

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
V_{VDD_ON}	VDD ON	T_J=25℃	7.3	8.2	8.8	V
V_{BS_ON}	VB_ON	T_J=25℃	4.3	5	6	V
V_{VDD_OFF}	VDD OFF	T_J=25℃	6.8	7.5	7.9	V
VCC	VCC pin voltage range	V_{VDD}=15V C_{VCC}=1uF	11.5	12.5	13.5	V
I_{STATE}	VDD quiescent current	V_{HI}=0V , V_{VDD}=15V, V_{BS}=12V		226	500	uA
I_{VDD}	VDD operating current	V_{VDD}=15V, F=250kHz, C_{HO}=1nF		4.3		mA
V_{HIH}	Input rising threshold		2.5	2.9	3.1	V
V_{HIL}	Input falling threshold		1.5	1.9	2.1	V
V_{HO+}	High level output voltage		11.5	VB-0.04	13.5	V
I_{HI+}	Input pull down current	V_{HI}=5V		66	200	uA
I_{HO+}	Peak source current	V_{BS}=12V, V_{HI}=5V	3.43	4.07	4.67	A
I_{HO-}	Peak sink current	V_{BS}=12V, V_{HI}=0V	3.21	3.87	4.52	A
T_{D_ON}	VHI rising to VHO rising	V_{VDD}=15V, V_{BS}=12V, C_L=1nF		42.7	100	ns
T_{D_OFF}	VHI falling to VHO falling	V_{VDD}=15V, V_{BS}=12V, C_L=1nF		45.6	100	
T_R	Rise Time HO	V_{VDD}=15V, V_{BS}=12V, C_L=1nF		4.61	10	
T_F	Fall Time HO	V_{VDD}=15V, V_{BS}=12V, C_L=1nF		3.9	10	

REMARKS: The HI pin logic input signal can be processed normally only after the chip power supply pin VDD reaches the starting voltage V_{VDD}_ON

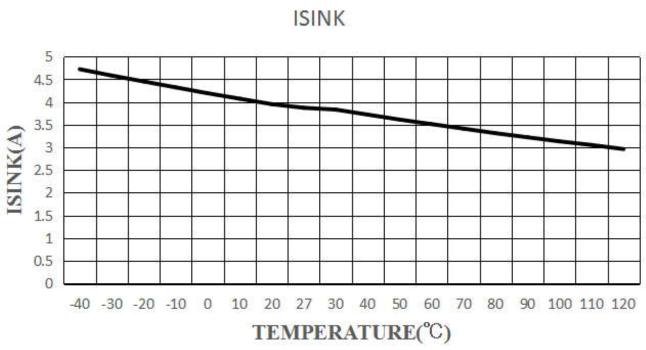


Figure1. HO pin peak sink current VS temperature

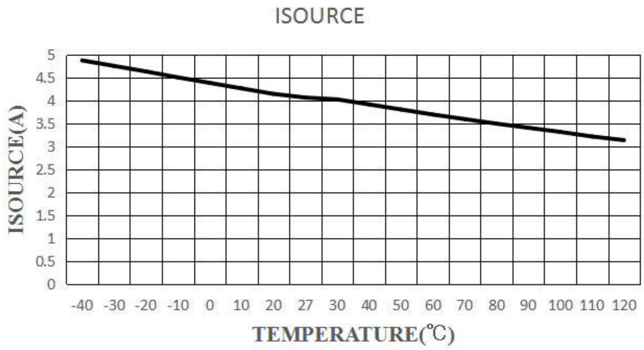


Figure2. HO pin peak source current VS temperature

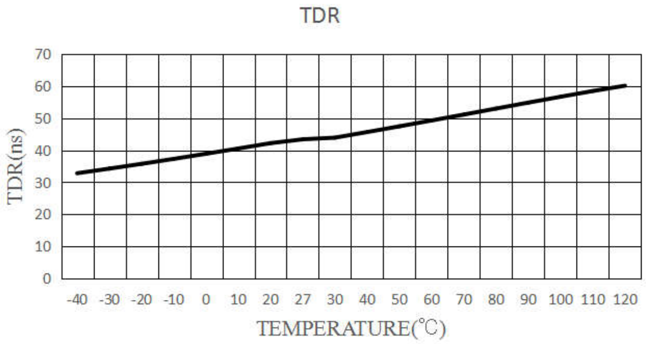


Figure3. VHI rising to VHO rising VS temperature

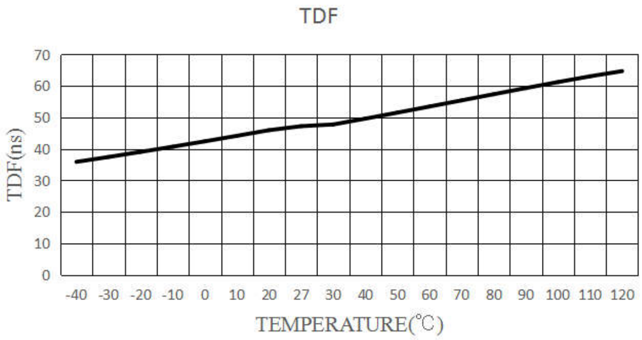


Figure4. VHI falling to VHO falling VS temperature

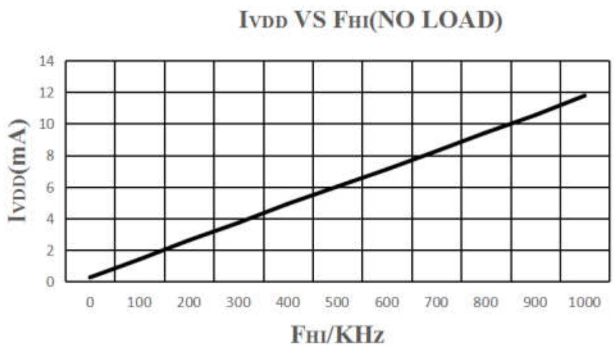


Figure5. Operating current VS operating frequency (VDD=15V)

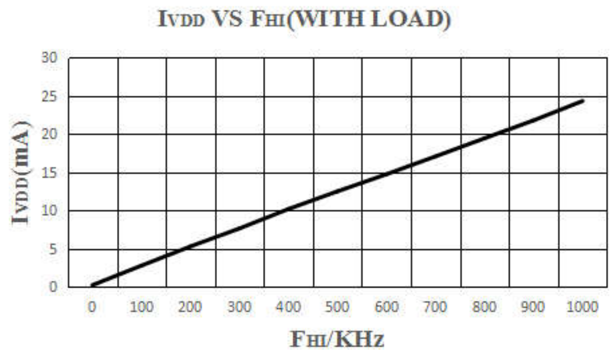


Figure6. Operating current VS operating frequency (VDD=15V 1nF LOAD)

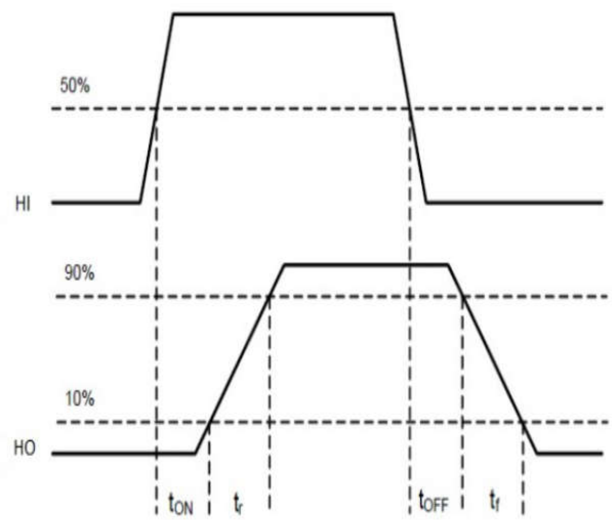


Figure7. Propagation Delay, Rise and Fall Times

PARAMETER MEASUREMENT INFORMATION

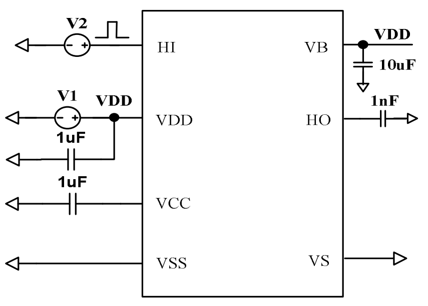


Figure8. Schematic diagram of the functional curve test circuit

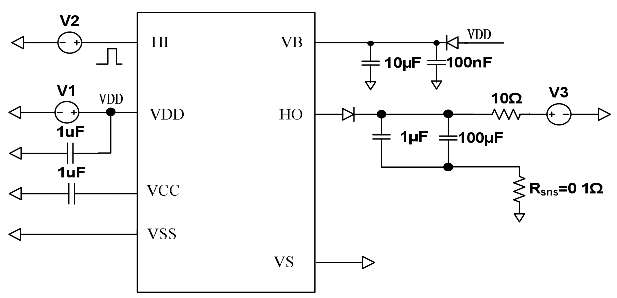


Figure9. Peak source current of the HO pin

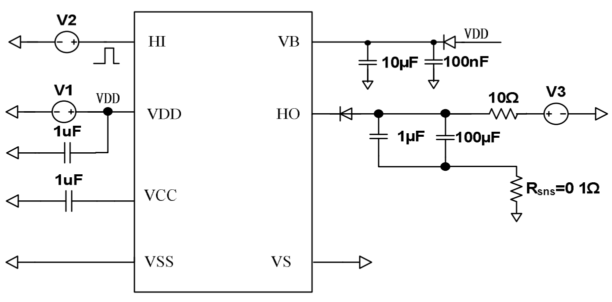


Figure10. Peak sink current of the HO pin

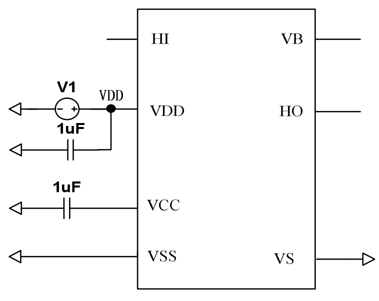


Figure11. The VCC pin output voltage

PRODUCT WORKING MODE

SCM3504C is a high side gate driver that can translate the logical pulse signal received by the HI pin to the voltage domain of V_{VS} ~ V_{VB}, and then output the corresponding drive signal through the HO pin to control the switch of the NMOS on the high voltage side. In the high voltage bootstrap applications, the pulse signal received by SCM3504C HI pin generally comes from the main control chip. The main control chip outputs the regular duty cycle signal according to the loop to control SCM3504C. SCM3504C restores the duty cycle signal of the main control chip at the HO pin to control the switch of the NMOS on the high voltage side.

UNDER VOLTAGE LOCK

The sequence is that the SCM3504C is enabled firstly, then the main control chip is enabled, and outputs the duty cycle signal. The HI pin of SCM3504C directly or indirectly connects with the duty cycle signal, and shifts to the V_{VS}~V_{VB} voltage domain, and restores the duty cycle signal at the HO pin.Therefore, the enable voltage and under voltage lockout voltage of SCM3504C are lower than that of the main control chip respectively, so that the performance of the main control chip will not be affected.

When the VDD pin voltage is less than 8.2V, SCM3504C does not process the signal of the HI pin; When the VDD pin voltage is greater than 8.2V and the V_{BS} is greater than 5V, SCM3504C outputs the drive signal in the same phase with the HI pin. The under voltage lockout voltage hysteresis is 0.7V, that is, when the VDD pin voltage drops from 8.2V to 7.5V, SCM3504C does not process the signal of HI pin.

HIGH VOLTAGE BOOTSTRAP

The SCM3504C V_{DD} pin can be connected together with the power supply terminal of the main control chip, or using other connection methods. Here to take a typical application circuit as an example of high-voltage bootstrapping work description.

Assuming that the normal operating voltage of the main control chip is 17V, when the charging circuit charge the VDD bypass capacitor from 0V to 17V, SCM3504C and the main control chip are enabled in sequence, during the sequence, all nodes of the system are initialized to 0V by default, that is, V_{VS}=0 V. The VDD voltage reaches the operating voltage of the main control chip, the main chip drives the low side NMOS on and the high side NMOS off ; the VS voltage follows the drop, VS≈0V (low side NMOS voltage drop and current sampling resistance voltage drop), VCC charges the bootstrap capacitor through the high voltage isolation diode, at V_{VDD}=17V, V_{BS}=12V. Ignoring the start delay, at V_{VDD}=17 V, the main chip drives the low side NMOS off, and the G_{TH} pin of the main control chip starts to output the duty cycle signal and send it to SCM3504C. SCM3504C restores the duty cycle signal in the V_{VS}~V_{VB} voltage domain, SCM3504C drivers the NMOS on the high voltage side on; VS voltage begins to rise and gradually equals V_{VIN} ; Due to the inability of capacitor voltage to suddenly change, so V_{BS} is still equal to 12V, and the NMOS on the high voltage side is fully on. At this time, V_{VB}=V_{VIN}+V_{BS}. During the whole working process, the relative voltage of SCM3504C is V_{BS}=12 V, which fully meets the withstand voltage requirements of the device, so the chip will not be damaged.

LEVEL SHIFT

After SCM3504C starting to receive the signal of HI pin, SCM3504C generates the set and reset signals when the HI pin signal appears rising edge and falling edge, respectively, in order to shift the HI pin signal to the V_{VS}~V_{VB} voltage domain, and then amplify the drive current to drive the NMOS on the high voltage side to complete energy conversion.

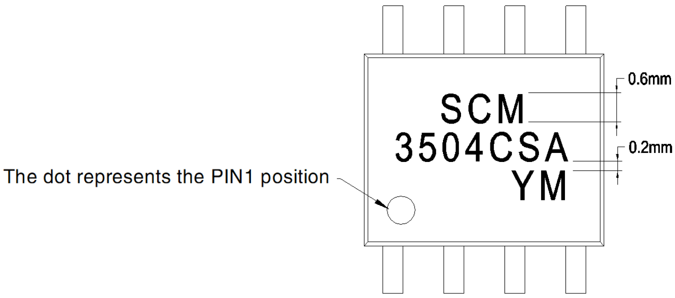
The difficulty of the level shift lies in how to filter out the influence of the switch noise and interference on the shift circuit at the moment of the NMOS switch on the high voltage side. SCM3504C with highly matched difference structure can effectively avoid the influence of common mode noise on the circuit.

ORDER INFORMATION

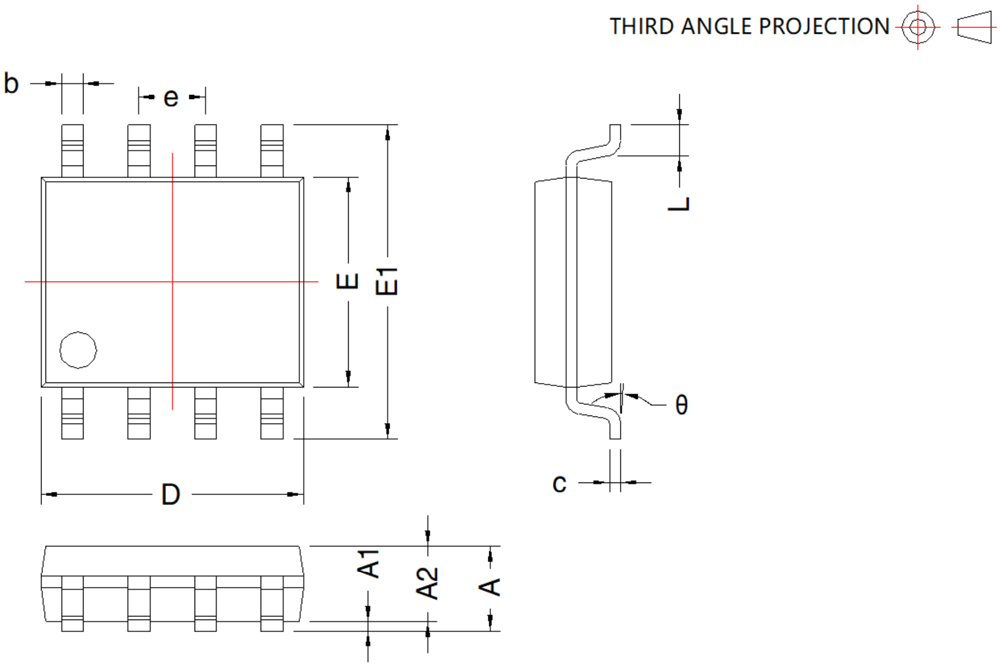
Product Model	Package	Pin Number	Silk-Screen	Pack
SCM3504CSA	SOP-8	8	SCM3504CSA YM	4K/Tray

Product model number and screen printing instructions
SCM3504XYZ:
(1) SCM3504, Product code.
(2) X = A-Z, Version code.
(3) Y = S, Package code; S: SOP package.
(4) Z = C, I, A, M, Temperature level code; C: 0℃-70℃, I: -40℃-85℃, A:-40℃-125℃, M: -55℃-125℃.
Silk-screen:
(5) YM: Product trace ability code; Y Product production year code, M Product production month code.

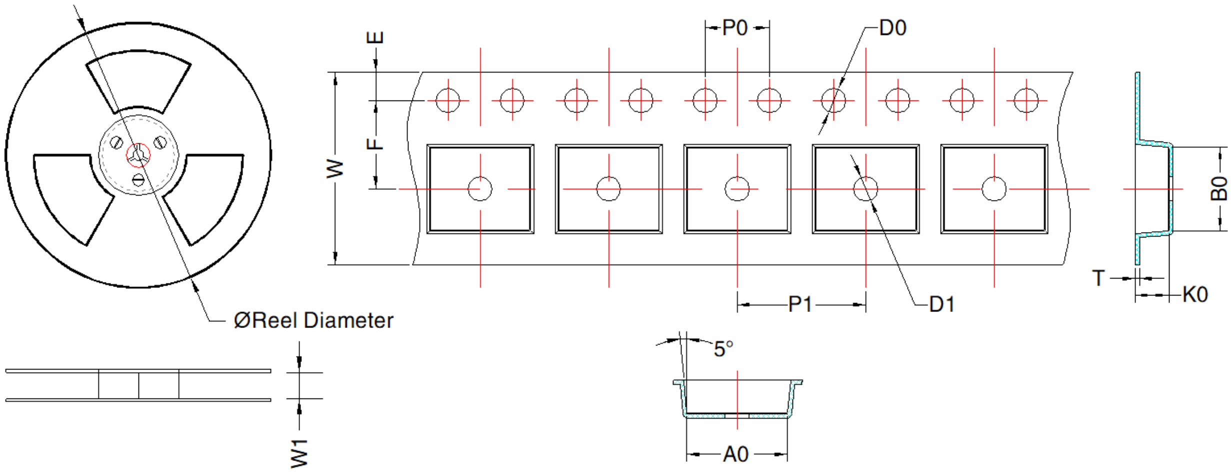
SILK PRINTING INFORMATION



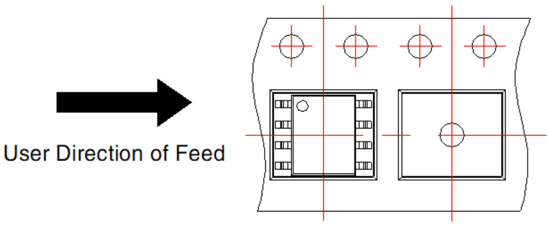
Note:
1、Typeface: Arial;
2、Character size:
Height: 0.6mm, Spacing: 0.1mm, LineSpacing: 0.2mm;



SOP-8				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	1.45	1.75	0.057	0.069
A1	0.10	0.25	0.004	0.010
A2	1.35	1.55	0.053	0.061
D	4.70	5.10	0.185	0.201
E	3.80	4.00	0.150	0.157
E1	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.50
b	0.33	0.51	0.013	0.020
e	1.27BSC		0.05BSC	
c	0.17	0.25	0.007	0.010
θ	0°	8°	0°	8°



The orientation of IC in tape



Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)
SCM3504CSA	SOP-8	3000	330.0	12.4	6.4 ± 0.1	5.4 ± 0.1	2.1 ± 0.1	0.25 ± 0.03	12.0 ± 0.3	1.75 ± 0.1	5.5 ± 0.1	8.0 ± 0.1	4.0 ± 0.1	1.5 ± 0.1	1.5 ± 0.1

Note: The minimum order quantity is the minimum packaging quantity, and the order quantity must be an integer multiple of MPQ.

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