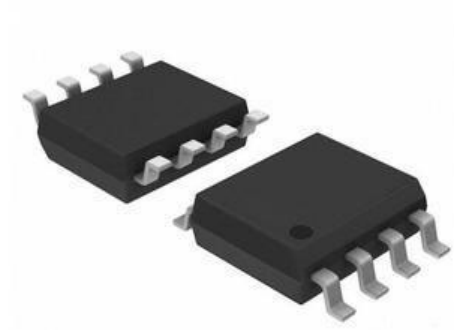
MORNSUN®

SCM1707A ACDC Two-Stage Optocoupler Feedback PWM Controller

Features

- Ultra-wide voltage input 18VDC~305VAC
- Including front-stage control and back-stage control
- Front-stage PWM control, frequency reduced under light load
- Front-stage jitter frequency function
- Back-stage jitter frequency function
- Frequency reduced under light load of back-stage. The frequency drops to 2.5 kHz when approaching no-load
- Built-in loop compensation
- Current limit per cycle
- VDD over-voltage protection and under voltage lockout
- Built-in over-current protection time
- Output over-voltage protection
- Open-loop and output short-circuit protection
- Bus over-voltage protection

Packaging



Optional package: SOP-8. Please refer to "Order Information" for screen printing information

Application

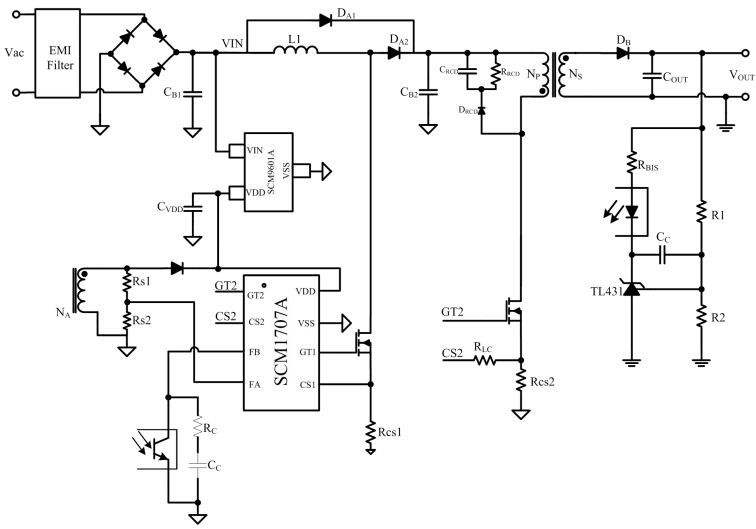
- Isolated AC-DC converter

Description

SCM1707A is an ACDC two-stage secondary feedback PWM controller, suitable for off-line two-stage flyback converter controlled by optocoupler feedback. The chip includes two independent loops for control: the front-stage and the back-stage. For the front-stage, after receiving the output voltage information fed back by the auxiliary winding through the built-in error amplifier, the front-stage power switch frequency and peak current amplitude are adjusted to stabilize the bus voltage. The front-stage, equipped with the built-in oscillator with a working frequency of 90 kHz, provides a jitter frequency function. The back-stage permits the PWM loop control through optocoupler feedback, and provides constant current function after soft start and before the output voltage reaches the set value. The constant current control adopts a control mode of "TDS/T=constant" to obtain high constant current precision. Constant voltage control adopts PWM+PFM mode, in which the additional jitter function reduces the output voltage ripple, the high power efficiency improves the EMI performance, and the frequency modulation control allows a small output ripple. Inside the IC, the working frequency of the back-stage can be trimmed to high precision. There is no working clock oscillator for the chip, and the maximum working frequency of the chip is determined by the peripheral inductance parameters to facilitate a convenient frequency adjustment.

In addition, a series of protection functions are integrated inside the chip to improve the reliability of the system, including output over-voltage protection (OVP), VDD over-voltage protection, VDD under voltage lockout, output short-circuit protection,Over-current protection per cycle,Over-temperature protection,back-stage input over-voltage protection and so on.All the protection functions can be automatically restored.

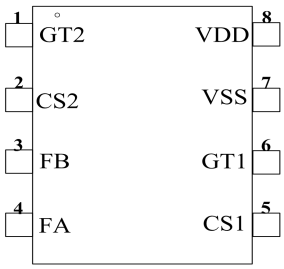
Typical Application Circuit



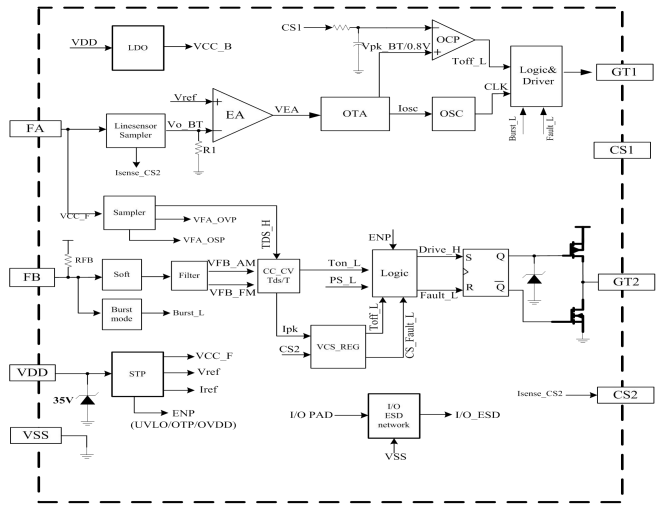
Typical application circuit Ultra-wide voltage AC input

Contents

Pin Configuration



Inter Block Diagram



Pin Description

No.	Name	I/O	Description
1	GT2	O	The back-stage is externally connected with MOSFET driving port
2	CS2		The flyback-stage current sampling pin, connected with the external sampling resistor to ground
3	FB	I	Voltage feedback pin. It forms loop feedback through optocoupler and generates PWM&PFM control signal together with current sampling pin (CS2)
4	FA	I	Input pin for timing feedback. This pin is connected to a voltage divider between an auxiliary winding and ground, and the upper resistance of the voltage divider can be used to adjust the feedforward compensation strength of the converter. Sampling the Boost output voltage by auxiliary winding, combined with the EA, the front-stage boost control loop may be achieved. Input over-voltage protection is designed
5	CS1	I	Front-stage Boost current sampling pin, connected with the external sampling resistor to ground
6	GT1	O	Front-stage external MOSFET driving port
7	VSS	P	Chip GND
8	VDD	P	Chip power port

Absolute Maximum Ratings

General test conditions: Free-air,normal operating temperature range (unless otherwise specified).

Parameter	Symbol	Min	Max	Unit
Bias power voltage	V_{VDD}		36	V
VDD clamp current	I_{CLAMP}		10	mA
GATE pin voltage	V_{GT1},V_{GT2}	-0.6	36	V
Voltage range	FA,FB,CS1,CS2	-0.6	6.6	
Storage temperature	T_{STG}	-55	150	℃
Soldering Temperature (Allowable reflow soldering temperature of chip within 10 seconds)			260	
Moisture sensitivity level	MSL	MSL3		
Electrostatic discharge (ESD) rating	Human Body Model (HBM)		1000	V
	Charging Equipment Model (CDM)		1000	

Note: Exceeding the stress values listed in the "Limit rating" table may cause permanent damage to the device. The reliability of the device may be affected when working under the limit rated condition for a long time. All voltage values are based on the GND.

Recommended Operating Conditions

Unless otherwise specified,the following are measured in the conditions of V_{VDD}= 12V.GT1,GT2=No Load

Parameter name	Symbol	Min	Max	Unit
Bias power voltage	V_{VDD}	15	24	V
VDD bypass capacitor	C_{VDD}	10	47	uF
Working frequency	F_{OSC}	65	110	kHz
Working junction temperature	T_J	-40	125	ºC

Electrical Characteristics

Unless otherwise specified,the following are measured in the conditions of V_{VDD}= 12V.GT1,GT2=No Load

Symbol	parameter	Test condition	Min	Typ	Max	Unit
Supply Section (VDD pin)						
I_{START_UP}	VDD starting current	V_{VDD}=8V, testing the current flowing into the VDD port		0.15	0.6	mA
I_{VDD_OP}	Chip working current	V_{FB}=3V		3.5	5	mA
I_{STATE}	Static working current of controller	Continue to step up to GT2 after VDD starts No output pulse, observing the current flowing into VDD port		1.2	1.8	mA
V_{UVLO_ON}	VDD under voltage lockout cancelled (starting)	VDD: low ~ high	13.5	14.7	15.9	V
V_{UVLO_OFF}	VDD under voltage lockout	VDD: high ~ low	7.45	8.1	8.75	
V_{VDDOVP_ON}	VDD over-voltage protection trigger voltage	VDD: low ~ high	21.2	23.1	24.9	V
V_{VDDOVP_OFF}	VDD over-voltage protection cancellation voltage	VDD: 25V~10V, V_{FB}=3V	14.1	15.4	16.6	V
V_{VDDOVP_HYS}	VDD over-voltage protection hysteresis voltage	VDD: 25V~10V, V_{FB}=3V		7.7		
V_{CLAMP}	VDD clamp voltage			30		V
Output voltage sampling pin (FA pin)						
V_{FA_NC}	FA pin negative clamp voltage	FA pin output current is 300uA		-50		mV
V_{FA_OVP}	FA pin over-voltage protection threshold voltage	Enter the test state, apply voltage to FA pin	3.9	4.3	4.7	V
K_{LC}	Feedforward compensation current to input current ratio	FA pin current output/CS pin current output		32		A/A
Feedback voltage input Section (FB pin)						
K_{AM}	PWM control rate	$\Delta V_{FB}/\Delta V_{CS}$		4		V/V
V_{FB_OPEN}	FB open-circuit voltage			5.4		V
I_{FB_SHORT}	FB short circuit current	Current when FB is grounded	0.22	0.31	0.4	mA
V_{FB_OLP}	Output short circuit protection threshold			4.5		V
Z_{FB_IN}	FB input resistance			15		Kohm
V_{TH_FBUVP}	FB under voltage protection threshold			1.8		V
V_{HYS_FBUVP}	FB under voltage protection hysteresis			0.4		V
Current sense inputs (CS1 and CS2 pins)						
V_{CS1T_MAX}	Built-in over-current protection threshold			0.8		V
V_{CS2T_MAX}	Built-in over-current protection threshold			0.8		V
K_{DE}	Maximum ratio of degaussing time/switch cycle	V_{FA}=3.5V (Measured from the system)		0.6		s/s
T_{CS_LEB}	Leading edge blanking time	GT2 continuous output. Apply 1V voltage to CS		230		ns
Oscillator Section (built-in oscillator in front-stage and watchdog in back-stage)						
F_{OSC}	Front-stage oscillator frequency	FA and FB suspending, CS1 grounding	70	90	110	KHz
F_{OSC_MIN}	Minimum working frequency of front-stage oscillator	FA pin pumping 2.5mA current		27		kHz
F_{JITTER}	Jitter frequency of front-stage oscillator			160		Hz
$\Delta F/F_{OSC}$	Jitter range of front-stage frequency		-3		3	%
ΔF_{TEMP}	Temperature stability of front-stage frequency	-40 ºC～125 ºC		2		%
ΔF_{VDD}	Variation of front-stage frequency with VDD	V_{VDD}=9~20V		2		%
D_{MAX}	Maximum front-stage duty cycle	CS1 grounding	76	84	92	%
F_{ST}	Back-stage starting frequency	FB suspending	19.1	21	22.9	kHz
F_{MIN}	Minimum back-stage working frequency	FB: 3V to1V		2.5		kHz
T_{ON_MAX}	Maximum back-stage turn-on time	CS2 grounding	10	12	14	us
Driving Section (GT1, GT2 pins)						
V_{GCL}	GATE clamp voltage	V_{VDD}=18V，C_{GATE}=1nF		15		V
T_R	Output rise time	C_{GATE}=1nF		180		nSec
T_F	Output falling time	C_{GATE}=1nF		30		nSec
Timing						
T_{D_OPP}	Overpower protection delay	CS=2V		3*T_{SW}		Tsw
T_{PD}	Over-voltage protection or over-temperature protection delay	V_{FA}>4.3V or T_J>150ºC		6*T_{SW}		Tsw
T_{J_SHUT}	Thermal shutdown temperature	Internal junction temperature		150		℃
$T_{J\_RESTART}$	Restart temperature	Internal junction temperature		100		℃
T_{D_PL}	Overpower protection delay	V_{FB}>4.5V		74		ms
T_{SLEEP}	Overpower protection \ output short circuit protection rest time	V_{FB}>4.5V		786		ms

Typical Performance Curves

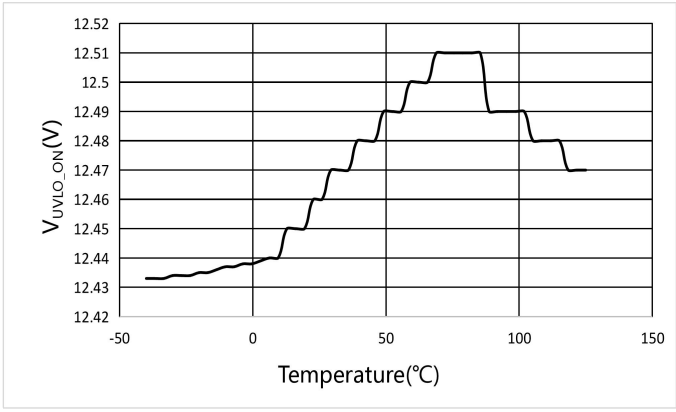


Fig. 1 VDD under voltage lockout cancellation voltage (starting) VS temperature

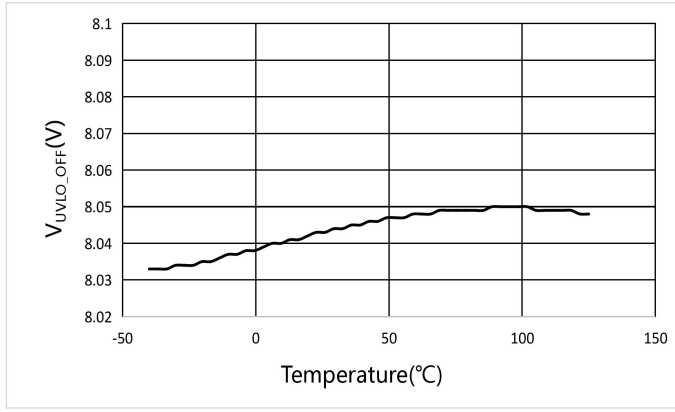


Fig. 2 VDD under voltage lockout VS temperature

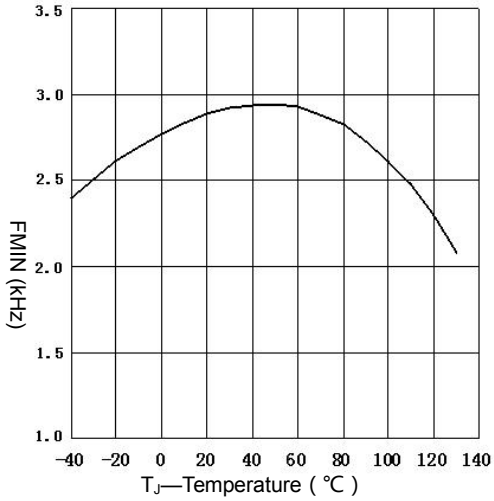


Fig. 3 Minimum switching frequency VS temperature

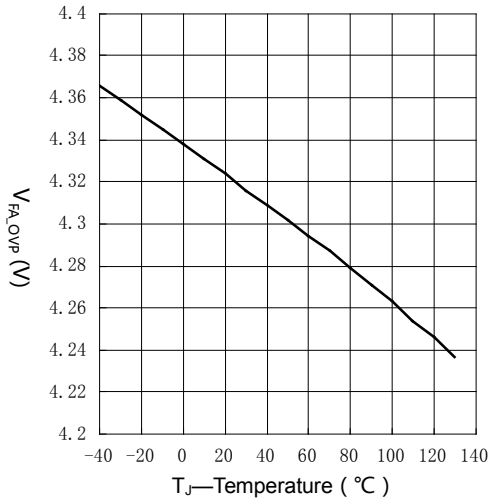


Fig. 4 FA overvoltage protection threshold VS temperature

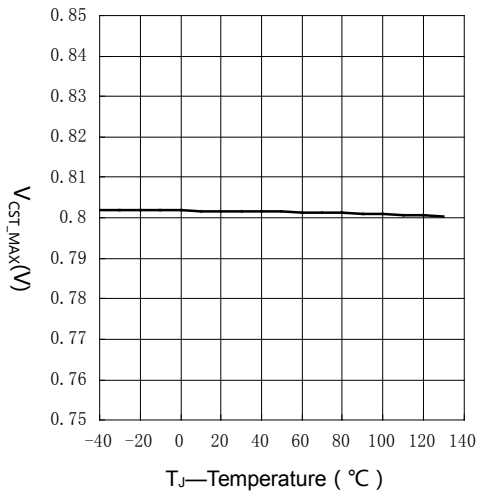


Fig. 5 Maximum CS threshold voltage VS temperature

Chip Overview

SCM1707A is an ACDC two-stage secondary feedback PWM controller, suitable for off-line two-stage flyback converter controlled by optocoupler feedback. It has three major characteristics. First, the chip contains two independent loops for control: the front-stage and the back-stage. For the front-stage, after receiving the output voltage information fed back by the auxiliary winding through the built-in error amplifier, the front-stage power switch frequency and peak current amplitude are adjusted, while the back-stage completes PWM loop control through optocoupler feedback. Second, under the condition of light load, the analog signal frequency is reduced with the decrease of load, improving the efficiency of light load. When it is close to no load, the frequency of the back-stage is reduced to the minimum working frequency, minimizing the standby power consumption. The third is the highly integrated protection function. There are few peripheral devices, reducing the area of PCB and ensuring consistent reliability.

Unless otherwise specified, the values shown below are typical values for V_{VDD}=12V test at normal temperature and pressure.

Built-in management clock

There is no working clock oscillator at the back-stage of the chip, and the maximum working frequency of the chip is determined by the peripheral parameters, so the frequency is easy to adjust. It is recommended that the working frequency of the latter stage be between 65 kHz and 110 kHz (see recommended working parameters for details). To improve the reliability, a management clock is built into the chip to prevent the loop from entering the dead zone due to interference. The built-in management clock mainly limits the minimum starting frequency of the chip flyback-stage to about 21 KHz, and the minimum working frequency is about 2.5K Hz in constant voltage mode. These two frequencies are also the timing basis of internal fault protection.

An oscillator is built in the front-stage of the chip, with a full-load working frequency is 90kHz, and it can realize jitter to spread the energy to a wider range than the bandwidth of the EMI tester, thus reducing EMI. At light load, the front-stage frequency is reduced, and the minimum working frequency is 27 kHz. For the back-stage, the jitter is realized by changing the Tring time. The jitter range of the front-stage and back-stages is set to 3% of the maximum frequency, and the jitter period is 6 ms. Schematic diagram of front-stage jitter is shown in the figure.

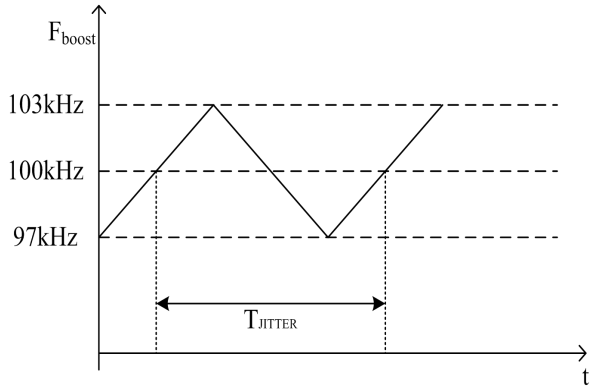


Fig. 6 Front-stage jitter diagram

Design of overcurrent point

The maximum ratio of transformer degaussing time T_{DEM} to switching period T_{SW} is set for SCM1707A. Therefore, according to the principle that the output current is equal to the average inductor current, the maximum output current (also called overcurrent point) I_{O_MAX} of the converter satisfies the following equation:

$$I_{O\_MAX} = \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot K_{DS} \cdot \eta_{XFMR} \cdot I_{PEAK\_MAX} \quad (1)$$

Where:

N_P/N_S: Transformer's turn ratio of primary/secondary side

K_{DS}: Maximum ratio of transformer T_{DEM}/T_{SW} (see electrical characteristics);

η_{XFMR}: Power conversion efficiency from the primary side to the secondary side of the transformer;

I_{PEAK_MAX}: Maximum peak current of primary side of transformer

So the overcurrent point can be designed by adjusting the transformer's turn ratio of primary/secondary side (N_P /N_S) and the maximum peak current I_{PEAK_MAX}.

In the constant current operation mode (VFB>3.4V), the controller is able to set the ratio of transformer degaussing time to switch cycle as K_{DS}, and the constant current point will become constant when the transformer parameters and maximum peak current are set. The maximum peak current is the maximum CS threshold voltage V_{CST2_MAX} (refer to electrical characteristics) divided by the current detection resistor R_{CS2}, as follows:

$$I_{PEAK\_MAX} = \frac{V_{CST2\_MAX}}{R_{CS2}} \quad (2)$$

Example: the core and winding loss of a transformer is 5%, the leakage inductance from the primary side to the secondary side is 3.5%, and the ratio of bias power to output power is 1.5%. The value of power conversion efficiency η_{XFMR} from primary side to secondary side of transformer is about: 1-0.05-0.035-0.015=0.9. To design a converter with output voltage of 5V, power of 3W, and required overload capacity of 10%, the turn ratio of primary/secondary side is 14. Then:

$$\begin{aligned} R_{CS} &= \frac{V_{CST\_MAX}}{2I_{O\_MAX}} \cdot \frac{N_P}{N_S} \cdot K_{DS} \cdot \eta_{XFMR} \\ &= \frac{0.8}{2 \times 0.66} \times 14 \times 0.6 \times 0.9 \quad (3) \\ &= 4.6\Omega \end{aligned}$$

The maximum front-stage peak current is the maximum CS threshold voltage V_{CST1_MAX} (refer to electrical characteristics) divided by the current detection resistor R_{CS1}, as follows:

$$I_{PEAK\_BT\_MAX} = \frac{V_{CST1\_MAX}}{R_{CS1}} \quad (4)$$

Built-in soft start

The flyback adopts built-in soft start, and the soft start current increases gradually in a continuous mode. Cause: to improve the startup waveform. If the secondary side of the soft-start current jump rises in a large step, the output voltage waveform also rises in a step when starting with full load.

Perform the soft start by controlling the gradual rise of V_{FB} voltage. Cause: to improve the starting overshoot (no resistance and capacitor are added on the secondary side to improve the starting overshoot). If the voltage of V_{FB} is not controlled, the coupler will not pump electric during startup, and the V_{FB} will be at the maximum potential. However, the loop is just established. Indeed the V_{FB} drops due to the pumping electric of the optocoupler, but there will be a certain delay, which may easily lead to overshoot. After soft start, V_{FB} is not limited by soft start circuit. Cause: the loop should not be affected after normal operation.

Both the first start and the restart after the end of protection can effectively initialize. Cause: assure that there is soft start for power-on start and restart after protection cancellation.

Intelligent FM green mode

SCM1707A may be able to adjust the frequency of oscillator by detecting F_B port voltage V_{FB}, that is, adjust the frequency of chip output signal GT2. When $3V<V_{FB}<3.4V$, the chip is in PWM mode, under which only the peak voltage of CS2 pin is adjusted, and the frequency is maximum and unchanged. When $1.9V<V_{FB}<3V$, the chip enters PWM+PFM mode, under which the peak voltage of CS2 and the working frequency of the chip are adjusted, and the frequency decreases gradually with the decrease of load. When $1.2V<V_{FB}<1.9V$, the chip enters PFM mode, under which the frequency gradually decreases to the minimum working frequency with the further reduction of load. When VFB is less than 1.2, the chip enters the minimum working frequency of 2.5 KHz. The curves of frequency, peak voltage and operation mode changing with V_{FB} are shown in Fig. 7.

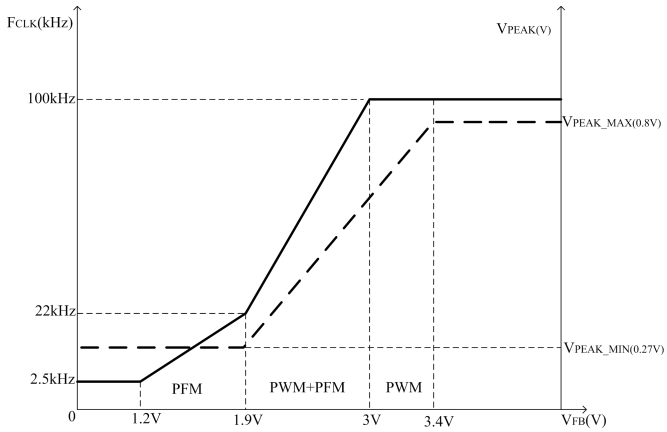


Fig. 7 Intelligent FM green mode

Feedforward Compensation

As illustrated in Fig. 8, the voltage waveform of the auxiliary winding is a periodic signal composed of three parts. The first part corresponds to the switching-on stage T_{ON}, when the voltage amplitude is about the converted value of the input voltage according to the turn ratio of the primary to the auxiliary side. The timing corresponding to the second part is the degaussing stage of the excitation inductor T_{DEM}, during which the voltage amplitude is about the converted value of the voltage at both ends of the secondary winding according to the turn ratio of the secondary to the auxiliary side. The timing corresponding to the third part is the primary inductance-capacitance resonance stage T_{RING}, during which the voltage amplitude is about the converted value of the primary resonance voltage according to the turn ratio of the primary to the auxiliary side.

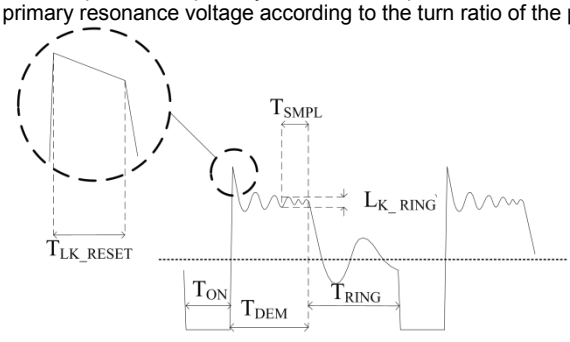


Fig. 8 Detailed information of auxiliary side signal waveform

Thus, the timing corresponding to the first part of the waveform is the switching-on stage, that is, the T_{ON} stage (see Fig. 8). According to the principle of flyback converter, the voltage on the auxiliary winding has a turn ratio relationship with the input voltage at this stage, in which the direction is opposite and the timing is completely separated from that of inflection point sampling, so the FA pin can be used to sample the input voltage at this stage (i.e., sample the bus voltage) to realize feedforward compensation. Combined with the error amplifier inside the chip, the steady-state control of bus voltage can be realized.

This method has been applied for patented. Simply speaking, NPN transistor is used to clamp the voltage of FA pin at this stage, that is, the emitter of NPN transistor is connected with FA pin, and the interior is controlled by logic, so as to provide bias voltage to the base of NPN transistor only when the switch tube is turned on. The magnitude of the bias voltage is about its turn-on junction voltage VBE. Then, when the negative voltage appears in the auxiliary winding, the NPN triode is turned on, and the FA pin outputs a current to "compensate" the negative voltage, so that the voltage of the FA pin is clamped at V_{FANC} (see electrical characteristics). This current is equal to the auxiliary side conversion value of the input voltage VVIN minus V_{FANC}, and then divided by the upper resistance of the voltage divider R_{S1}. Finally, this current is reduced according to the feedforward current ratio KLC (refer to the electrical characteristics), and then used as the feedforward compensation current I_{COMP} to generate the compensation voltage V_{RLC} on the feedforward resistance R_{LC}. Thus, the feedforward compensation current I C_{OMP} satisfies the following equation:

$$I_{COMP} = \frac{1}{K_{LC}} \cdot \frac{\frac{N_A}{N_P} \cdot V_{VIN} - V_{FANC}}{R_{S1}} \quad (5)$$

According to the feed-forward compensation principle, if the overcurrent points have little difference under high and low voltage input, the compensation voltage VRLC should satisfy the following equation:

$$V_{RLC} = I_{COMP} \times R_{LC} = \frac{V_{VIN} \times T_D}{L_P} \times R_{CS2} \quad (6)$$

Where:
T_D is the current detection delay including the switch-off delay;
L_P is the primary inductance of transformer;
Other parameters have been mentioned above.
The feedforward resistor RLC is designed with reference to equation (5)

Bus voltage Design

For the settings of steady-state value V_{O_BT} of boost output voltage and bus overvoltage point V_{OBT_OVP}, please refer to the following equations:

$$V_{O\_BT} = I_{RS1} \cdot R_{S1} \cdot \frac{N_P}{N_A} \quad (7)$$

$$V_{OBT\_OVP} = I_{RS1\_OVP} \cdot R_{S1} \cdot \frac{N_P}{N_A} \quad (8)$$

Where IRS1=2.08mA, IRS1_OVP=2.42mA.
It can be learnt that by setting the pull-up resistor RS1 of FA and the turn ratio of the primary side to the auxiliary winding, the front-stage output voltage and the front-stage output overvoltage point may be set.

Switching Frequency Design

Upon the design of the constant voltage point and overcurrent point, the maximum peak current I_{PEAK_MAX} and overcurrent point P_{O_MAX} are determined accordingly. The maximum switching frequency F_{SW_MAX} of the converter satisfies the following equation:

$$F_{SW\_MAX} = \frac{2 \cdot P_{O\_MAX}}{L_M \cdot I_{PEAK\_MAX}^2 \cdot \eta_{XFMR}} \quad (9)$$

Thus, the switching frequency can be designed by adjusting the excitation inductance L_M. It should be noted that the maximum frequency is limited inside the controller, and the maximum switching frequency that SCM1707A can provide is 178 kHz.

Front-stage Slope Compensation

Single-stage compensation mechanism is adopted. When the duty cycle of the front-stage output GT1 is 40%~85%, the slope is 200mV/us.

Fault protection

SCM1707A integrates a variety of protection functions, including:
Output short -circuit protection (OSP)
Output overvoltage protection (OVP)
Over-temperature protection for CS pin fault protection controller
VDD overvoltage protection

Output short -circuit

Refer to Fig. 9. Stage 1: when the output is short-circuited, the controller will not be able to obtain energy from the auxiliary winding to maintain normal operation. At this time, the voltage V_{VDD} of the capacitor C_{VDD} of externally connected to VDD pin will continue to drop, and the short-circuit protection timing T_{D_PL} (refer to electrical characteristics) is started inside the chip until $V_{VDD}=V_{UVLO\_ON}$ (refer to electrical characteristics). Nevertheless in this process, the controller will still have certain GT2 signal output.

Stage 2: when the short-circuit protection timing ends or $V_{VDD}=V_{UVLO\_ON}$, the controller stops outputting GT2 signal, and VDD continues to power down. In this process, the controller never outputs GT2 signal, so the power consumption of the controller is small, the falling slope of V_{VDD} is smaller than that of stage 1, and the corresponding time will increase.

Stage 3: Subsequently, the controller is reinitialized. The logic signal in the chip returns to the state before start, and the external startup IC starts charging C_{VDD} until $V_{VDD}=V_{UVLO\_OFF}$ (refer to electrical characteristics).

It can be seen that the converter can dissipate heat by using Stage 2 and Stage 3. If the output short circuit fault is still not eliminated after the end of Stage 3, the controller returns to Stage 1 to start a new cycle process, and the converter enters the "hiccup" mode. As shown in Fig. 9, Stage 2 is also called UVLO process.

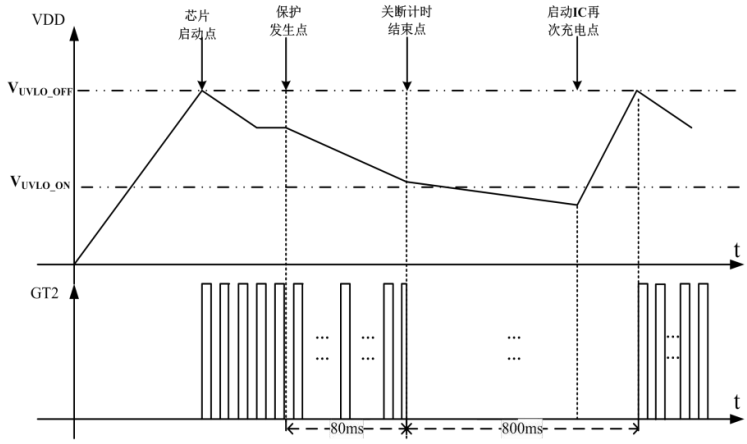


Fig. 9 Timing of output short-circuit protection related waveform

It should be noted that when the converter is overloaded, the output current cannot continue to increase due to the limitation of the over-current point, so the output voltage may have to decrease to ensure the constant output power and realize energy conservation. Therefore, under overload condition, only when the output voltage is as low as the lower limit value and the auxiliary winding cannot provide the energy to maintain the normal operation of the controller, the controller will be able to enter the working process similar to the above-mentioned stage 1, and the converter will be able to hiccup.

If the CS pin is suspended or the current stress of the current detection resistor R_{CS} is too large due to the output short circuit, so that $V_{CS}\geq V_{CSF}$ (refer to the electrical characteristics), then the controller will start timing; If the fault duration is equal to T_{D_OPP} (refer to electrical characteristics), the controller will stop outputting the driving signals GT1 and GT2, the auxiliary winding will not be able to provide energy to maintain the normal operation of the controller, and V_{VDD} will continue to drop. The specific working process of CS pin fault protection is the same as that of output over-voltage protection. Please refer to output over-voltage protection.

Output over-voltage protection

When the turn ratio is not selected properly in the process of testing single point fault or debugging the converter, the output voltage and the voltage on the auxiliary winding may be high, thus damaging the converter circuit and its load, and even damaging the controller. Output over-voltage protection is integrated in SCM1707A, so as to effectively avoid the above phenomenon.

Please refer to Figure 4. The method to realize output over-voltage protection is to generate a voltage signal V_{FAS} by sampling the inflection point voltage of FA pin, and when $V_{FAS}\geq V_{FA\_OVP}$ (refer to electrical characteristics), the controller starts timing. If the fault duration is equal to T_{PD} (refer to electrical characteristics), the controller will stop outputting the driving signal GATE, the auxiliary winding will not be able to provide the energy to maintain the normal operation of the controller, V_{VDD} will continue to drop, and the controller will enter the working process similar to the output short circuit protection stages 1~3. For the design of output over-voltage protection point, refer to the following equation:

$$V_{O\_OVP} = V_{FA\_OVP} \cdot \left(1+\frac{R_{s1}}{R_{s2}}\right) \cdot \frac{N_S}{N_A} - V_F \quad (10)$$

So the output over-voltage protection point can be adjusted by setting the turn ratio of the secondary side and the auxiliary winding, as well as RS1/RS2. Then the output over-voltage protection function can be started.

CS pin fault protection

If the CS pin is suspended or the current stress of the current detection resistor R_{CS} is too large due to the output short circuit, so that $V_{CS}\geq V_{CSF}$ (refer to the electrical characteristics), then the controller will start timing; If the fault duration is equal to T_{D_OPP} (refer to electrical characteristics), the controller will stop outputting the driving signals GT1 and GT2, the auxiliary winding will not be able to provide energy to maintain the normal operation of the controller, and V_{VDD} will continue to drop. The specific working process of CS pin fault protection is the same as that of output over-voltage protection. Please refer to output over-voltage protection.

Over-temperature protection

In order to protect the internal devices from over-temperature damage, the controller is provided with built-in over-temperature protection. When the junction temperature of the controller reaches T_{J_SHUT} (refer to electrical characteristics), the controller will start timing. If the fault duration is equal to T_{PD}, the controller will stop outputting the driving signals GT1 and GT2, the auxiliary winding will not be able to provide energy to maintain the normal operation of the controller, and VVDD will continue to drop. The specific working process of controller over-temperature protection is the same as that of output over-voltage protection. Please refer to output overvoltage protection.

Only when the junction temperature of the controller is lower than $T_{J\_RESTART}$ (refer to electrical characteristics), the controller overtemperature protection will be cancelled.

VDD pin over-voltage protection

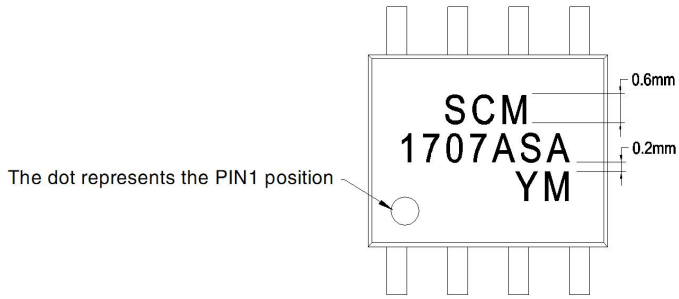
If the voltage at the VDD port exceeds 23.1V and lasts for 100us, the chip enters the VDD over-voltage protection state, and there is no signal output from the GATE. Only when the VDD voltage is less than 15.4V, the chip will cancel the VDD over-voltage protection signal, and then the GATE will resume normal output.

Ordering information

Product Model	Packaging	Quantity of Pin	Silk Screen	Packing
SCM1707ASA	SOP-8	8	SCM 1707ASA YM	3K/tray

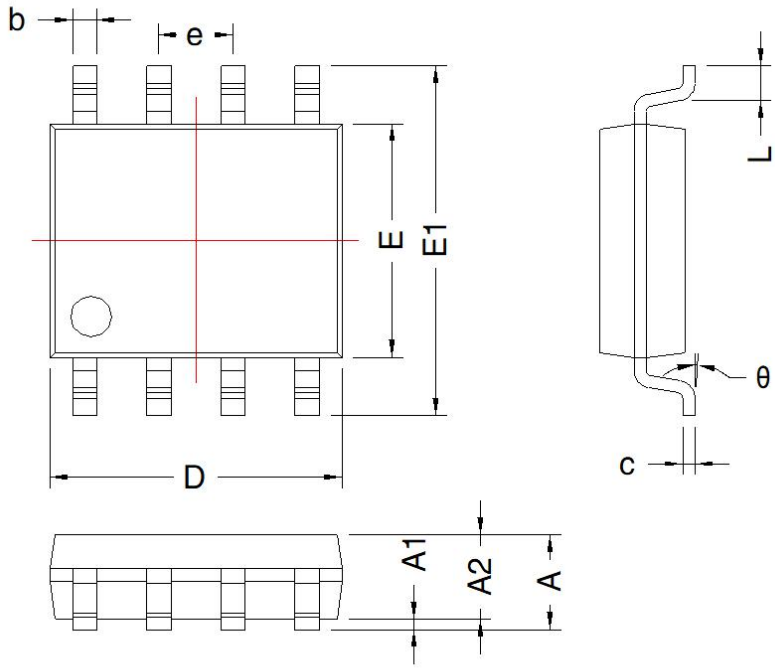
Product model number and screen printing instructions
SCM1707XYZ:
(1) SCM1707 = Product designation
(2) X = Version code information (A-Z)
(3) Y = Packaging definition code; S for SOP package.
(4)Z = Operating temperature range (C = 0℃ to +70℃, I =-40℃ to +85℃, A =-40℃ to +125℃, M = -55℃ to +125℃) .
(5) YM: Date code for product traceability; Y = code for production year; M = code for production month

Silk Screen Information

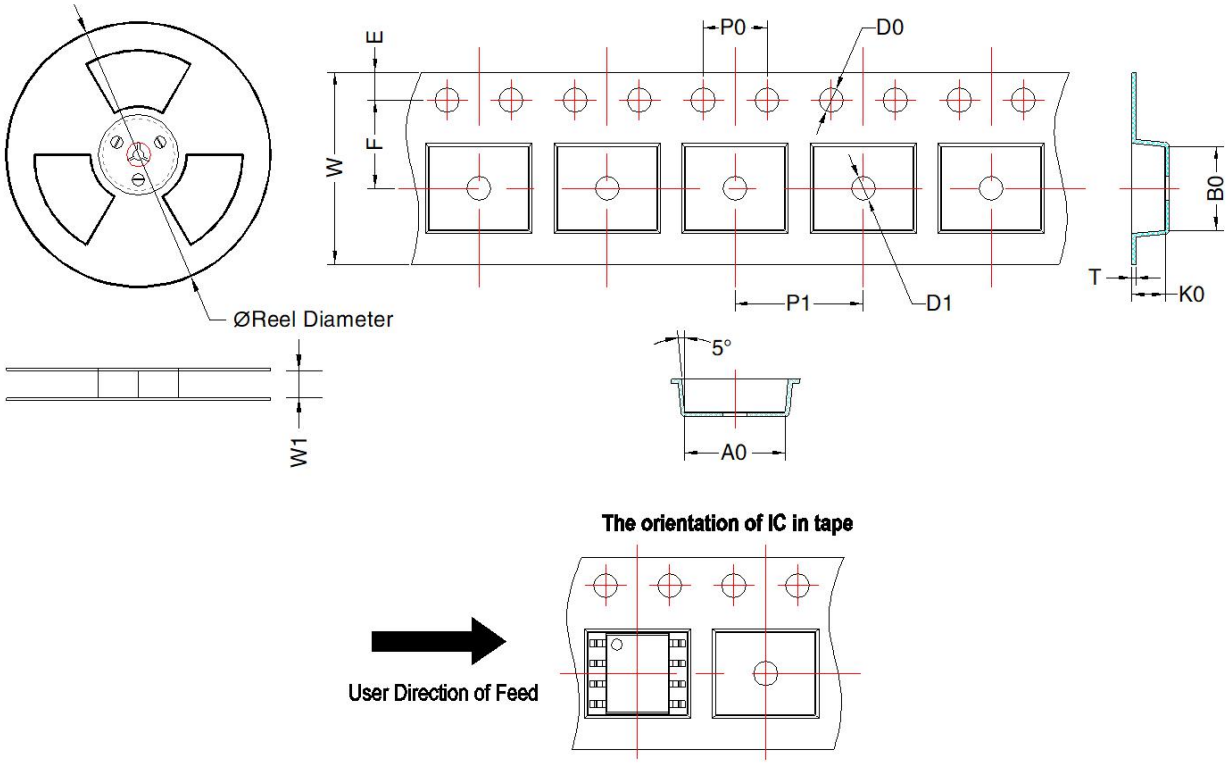


Note:
1、Typeface: Arial;
2、Character size:
Height: 0.6mm, Spacing: 0.1mm, LineSpacing: 0.2mm;

THIRD ANGLE PROJECTION



SOP–8				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.35	1.55	0.053	0.061
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
E1	5.80	6.20	0.228	0.244
L	0.40	0.80	0.016	0.032
b	0.33	0.51	0.013	0.020
e	1.27TYP		0.05TYP	
c	0.17	0.25	0.0067	0.001
θ	0°	8°	0°	8°



Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)
SCM1707ASA	SOP-8	3000	330.0	12.4	6.5 ± 0.2	5.45 ± 0.2	2.0 ± 0.2	0.3 ± 0.05	12.0 ± 0.3	1.75 ± 0.1	5.5 ± 0.1	8.0 ± 0.1	4 ± 0.1	1.5 ± 0.1	1.5 ± 0.1

Note: The minimum order quantity is the minimum packing quantity, and the order quantity shall be an integral multiple of MPQ.

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