MORNSUN®

SCM1102C Highly Integrated PWM Controller

Features

- Built-in soft start
- Minimum chip starting voltage 4V
- RI pin optional jitter frequency function
- Frequency Reduction at Light Load and Burst Mode Control under no load
- Programmable Maximum Switching Frequency
- Built-in slope compensation
- Built-in loop compensation
- Cycle-by-Cycle Current Limiting
- VDD over-voltage protection
- VDD under-voltage lockout
- Open loop and output short circuit protection
- Input under-voltage protection
- Built-in feed-forward compensation circuit

Package

Mechanical package: MSOP-8 see "Ordering information" for details)"

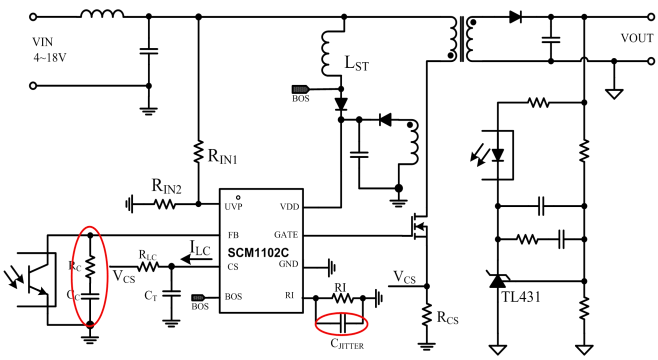
Applications

- DC-DC isolate Converter

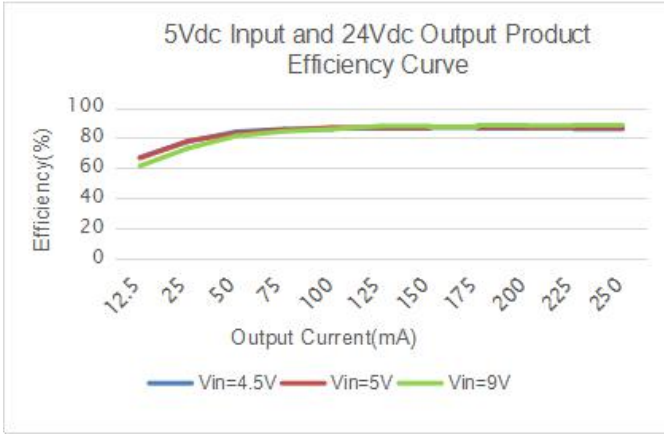
Functional Description

SCM1102C is a highly integrated current mode PWM controller, applicable to isolating DC-DC Converter. Inside the SCM1102C.The PWM switching frequency is internally adjusted within a tight range. It can change its maximum operating frequency by connecting with different resistors externally. Under light load, operating frequency of chip reduces with load decrease, thus allow Converter to maintain high efficiency within the whole load range. the power supply enters into a burst mode under no load conditions., which reduces standby power consumption greatly. Besides, a series of protective functions are integrated in the SCM1102C to improve system reliability, including VDD under-voltage lockout (UVLO), VDD over-voltage protection (OVP), open loop/output short circuit/overload protection (OLP), CS pin floating protection, input under-voltage protection. BOS pin externally connect with inductance to VIN and with diode to VDD to realize the minimum chip starting voltage, 4V.

Typical Application Circuit

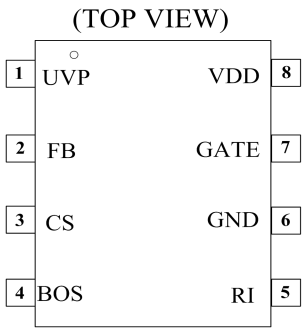


Functional Curve

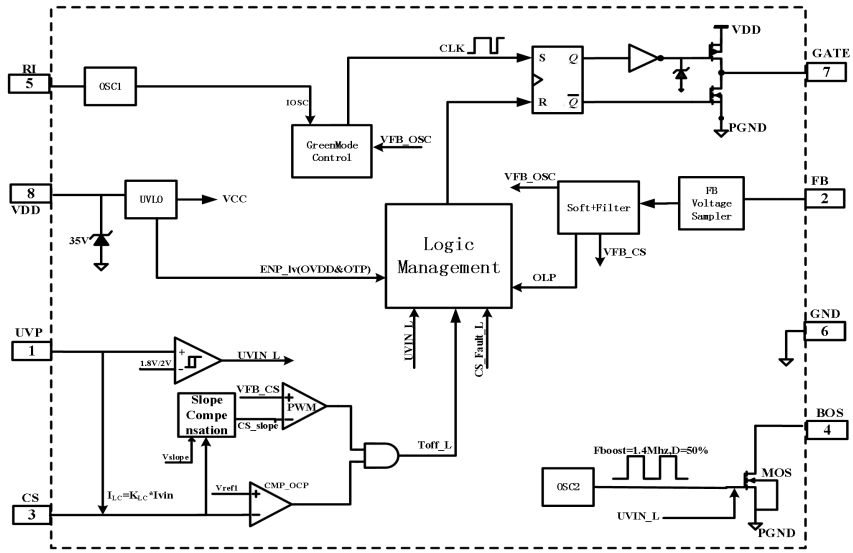


Contents

Pins



Internal Block Diagram



Pin Description

Number	Name	I/O	Description
1	UVP	I	Input voltage detect pin, DC input voltage connect divider resistance to UVP pin, adjust resistance on UVP pin will adjust feed-forward compensation current (resistance proportion can adjust input under-voltage point).
2	FB	I	Voltage feedback pin. It formulates feedback loop by opto-coupler and adjusts PWM signal duty ratio with current sampling (CS) signal.
3	CS	I	Current sampling input port
4	BOS	I	BOS pin connects inductance to input, then diode to VDD to realize BOOST function and low voltage 4V input. BOS pin is floating or earthed, enabling 9V~36V input.
5	RI	I	Set up maximum operating frequency for chip via externally earthed resistor. This external resistor in parallel with capacitor realizes frequency jittering and improves EMI performance.
6	GND	P	Chip reference ground
7	GATE	O	MOSFET drive port
8	VDD	P	Chip power supply port

Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (unless otherwise specified).

Parameter	Symbol	Minimum	Maximum	Unit
Bias supply voltage	V_{VDD}		35	V
VDD clamp current	I_{CLAMP}		10	mA
GATE pin voltage	V_{DRV}	-0.6	35	V
Voltage range	FB,CS,RI	-0.6	6	
	UVP	-0.6	6	
	BOS	-0.6	36	
Working junction temperature	T_J	-40	150	℃
Storage temperature	T_{STG}	-55	150	
Soldering Temperature (Allowable reflow soldering temperature of chip within 10 seconds)			260	
Moisture sensitivity level	MSL	MSL3		
Rated value of electrostatic discharge (ESD)	Human body model (HBM)		5000	V
	Charging device model (CDM)		1000	

Note: exceeding stress value listed in the “maximum rating” table may cause permanent damage to components. If working under extreme conditions for a long time, reliability of components may be affected. All voltage values is on the basis of GND.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit
Bias supply voltage	V_{VDD}	10	18	V
VDD Bypass Capacitor	C_{VDD}	1	20	μF
Operating frequency	F_{OSC}	220	500	kHz
Operating ambient temperature	T_A	-40	125	℃

Electrical Characteristics

Unless otherwise specified, the following parameters are measured under normal temperature normal voltage and in unsealed environment. V_{SS}=0V.

Symbol	Parameter	Test condition	Minimum	Typical	Maximum	Unit
Power Supply (VDD pin)						
I_{START_UP}	VDD star-up current	V_{VDD}=6V,test current flowing into VDD port	230	290	350	μA
I_{VDD_OP}	Chip operating current	V_{FB}=3V,RI=24K	1.4	1.9	2.4	mA
I_{FAULT}	Input under voltage, VDD under voltage lockout or VDD over voltage protection current	After floating BOS and star-up, continue to increase VDD voltage untile GATE no output pulse, observe current flowing to VDD port	224	280	336	μA
V_{UVLO_ON}	Release VDD under voltage lockout (start)	VDD from low to high, BOS pin floats or be earthed	6.6	7.1	7.6	V
		VDD from low to high, BOS pin connects in series with 1kΩ resistance, then connect with 5V voltage	14.8	15.9	17	
V_{UVLO_OFF}	VDD under voltage lockout	VDD from high to low	5.7	6.15	6.6	V
V_{VDDOVP_ON}	VDD over voltage protection Threshold	VDD is 15V~25V,V_{FB}=3V, BOS pin floats or be earthed	20.4	22	23.6	V
V_{VDDOVP_OFF}	VDD over voltage OFF voltage	VDD is 25V~10V,V_{FB}=3V BOS pin floats or be earthed	14.5	15.6	16.7	V
V_{VDDOVP_HYS}	VDD over voltage protection hysteresis			6.4		V
V_{CLAMP}	VDD clamping voltage	VDD absorption current increases suddenly	30	35	40	V
Input Voltage Detection pin (UVP pin)						
V_{UVP_OFF}	UVP pin input under-voltage protection voltage	R_{IN1}=500K,R_{IN2}=100K,RI=24K ,V_{IN}=12V~9V BOS pin floats or be earthed	1.71	1.8	1.89	V

V_{UVP_ON}	UVP pin input under-voltage release voltage	R_{IN1}=500K,R_{IN2}=100K,RI=24K ,V_{IN}=9V~14V BOS pin floats or be earthed	1.9	2	2.1	V
V_{UVP_HYS}	UVP pin input under-voltage hysteresis			0.2		V
V_{UVP_CLAMP}	UVP pin clamping voltage		2.23	2.4	2.57	V
K_{LC}	Feed-forward compensation current and input current proportion			5		
Feedback Voltage Input pin (FB pin)						
AV_CS	PWM input gain	$\triangle V_{FB}/\triangle V_{CS}$		3.67		V/V
V_{FB_OPEN}	FB open circuit voltage		4.95	5.36	6.05	V
I_{FB_SHORT}	FB short circuit current	Current when FB is earthed	1.05	1.28	1.57	mA
Z_{FB_IN}	FB input resistance			4.2		KΩ
V_{TH_PL}	FB over-voltage protection threshold value			4.54		V
V_{TH_FBUVP}	FB voltage threshold when entering Burst mode		0.93	1.1	1.27	V
V_{HYS_FBUVP}	FB voltage threshold return difference in Burst mode			0.25		V
V_{TH_FR}	Quick dynamic response threshold			0.7		V
Current Detection Input pin (CS pin)						
V_{CST_MAX}	Maximum limiting current threshold			0.8		V
K_{LC}	Feed-forward current proportion coefficient	I_{LC} / I_{IN}		5		
Low Voltage Start-up Function (BOS pin)						
V_{VDD_BOS}	VDD voltage required by BOS operation	BOS connects with 1k resistance, then to VDD		3.2	3.5	V
Oscillator (RI pin)						
F_{OSC}	Oscillator frequency	RI=24K、V_{FB}=3V	272	287	302	KHz
F_{JITTER}	RI pin frequency jittering	RI=24K,CI=2nF		145		Hz
$\triangle F/F_{OSC}$	Frequency jitter range		-6		6	%
$\triangle F_{TEMP}$	Temperature stability of frequency	–40℃ ~ 125℃		2		%
$\triangle F_{VDD}$	Frequency change with VDD	V_{VDD}=7~16V		2		%
D_{MAX}	Maximum duty ratio	CS be earthed, V_{FB}=4.5V	75	79	83	%
R_{RI_RANGE}	RI variation range		14	24	31	KΩ
V_{RI_OPEN}	RI open circuit voltage		1.9	2	2.1	V
F_{BM}	Operating frequency in BURST mode	V_{FB}=1.27V,RI=24K		120		KHz
Driving pin (GATE pin)						
V_{GCL}	GATE clamp voltage	V_{VDD}=18V,C_{GATE}=1nF		15		V
T_R	Output rise time	C_{GATE}=1nF		50		nS
T_F	Output fall time	C_{GATE}=1nF		35		nS
Time Parameters（TIMING）						
T_{D_OVP}	VDD over-voltage protection delay time			100		μS
T_{D_UVIN}	Input under-voltage protection delay time			70		μS
T_{D_OPP}	CS floating protection delay time	CS=2V,T_{SW} switching period		2*T_{SW}		
T_{D_PL}	Over-power protection delay time	RI=24K（calculate by F_{OSC}=287kHz）T_{OSC}=1/F_{OSC}		85.5(2457 6*T_{OSC})		mS
T_{SLEEP}	Over-power protection/open loop protection/VFB over-voltage protection sleeping time	RI=24K（calculated by F_{OSC}=287kHz）T_{OSC}=1/F_{OSC}		912.2(2^{18}* T_{OSC})		mS

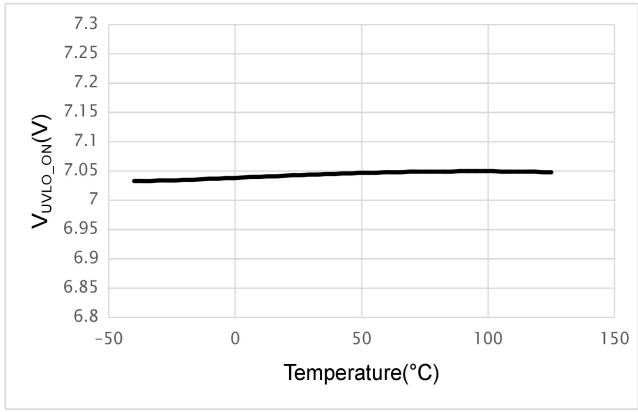


Fig. 1 VDD under-voltage revocation voltage (without Boost function) (start) VS Temperature

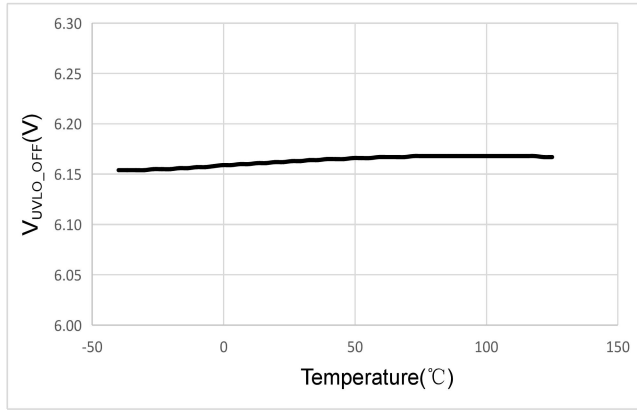


Fig. 2 VDD under-voltage locking VS Temperature

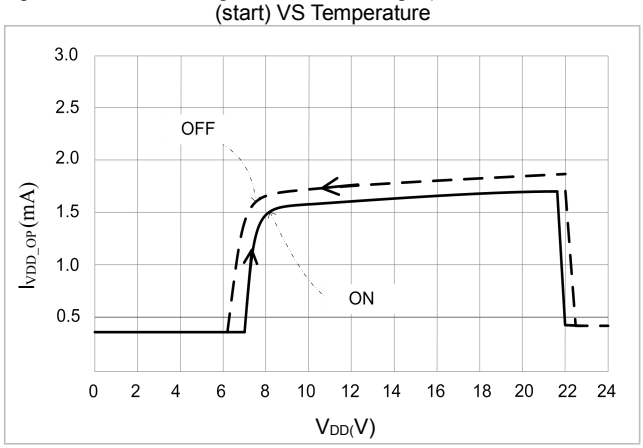


Fig. 3 Chip operating current VS VDD voltage

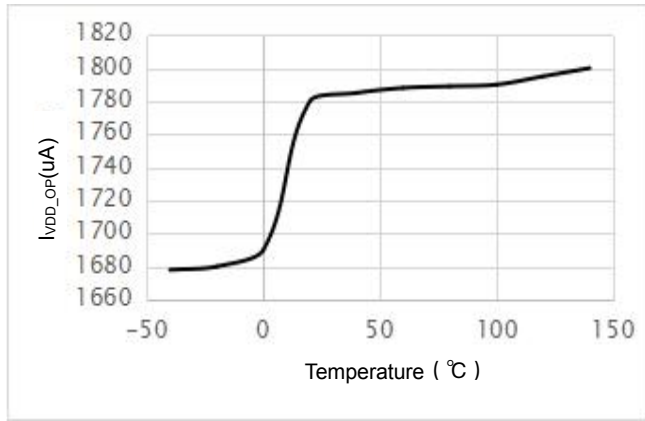


Fig. 4 Chip operating current VS Temperature

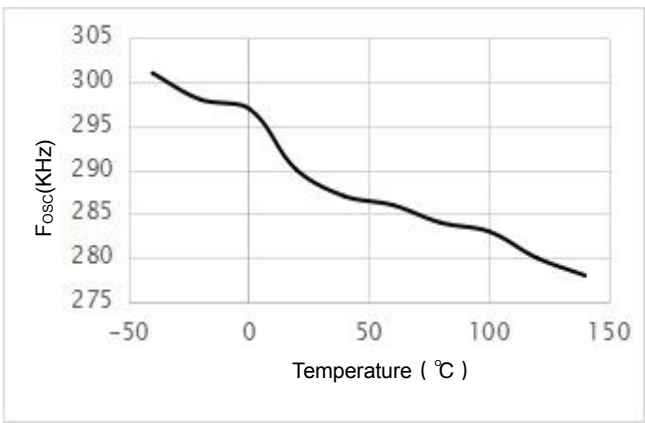


Fig. 5 Operating frequency VS Temperature

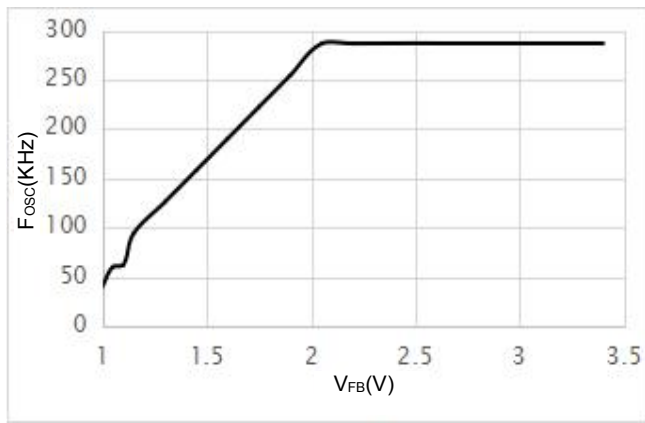


Fig. 6 Operating frequency VS V_{FB} voltage

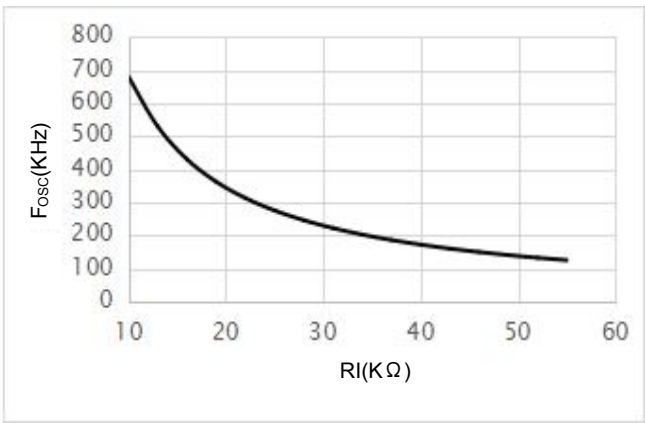


Fig. 7 Operating frequency VS RI pin resistance

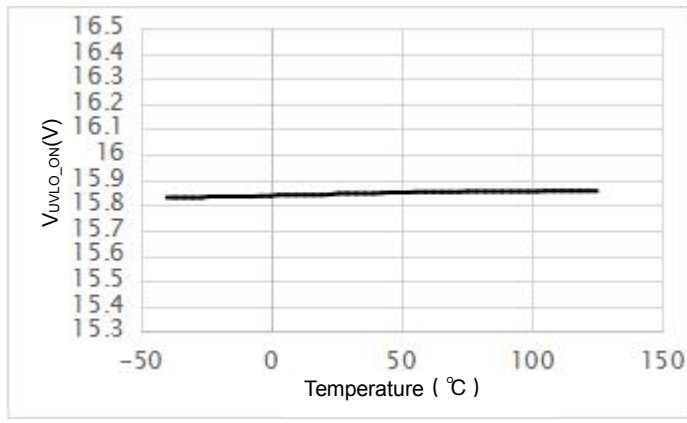


Fig. 8 VDD under-voltage lockout release voltage when Boost is working VS Temperature

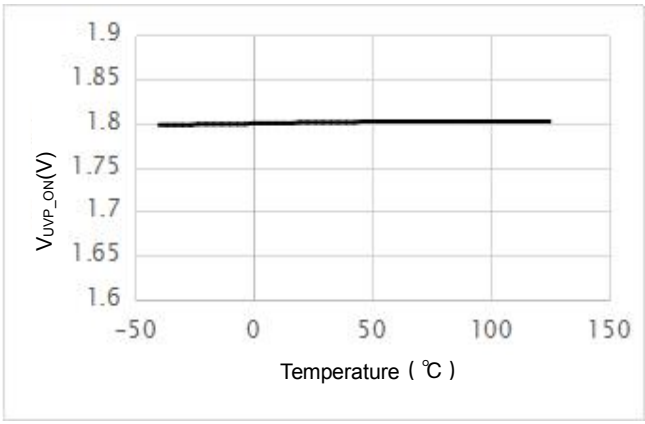


Fig. 9 UVP pin input under-voltage protection voltage VS Temperature

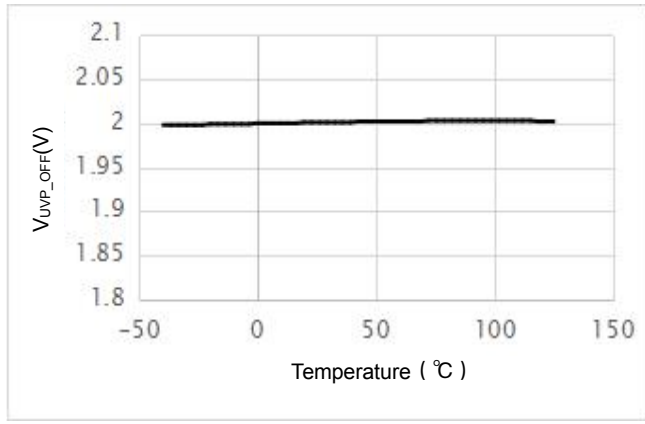


Fig. 10 UVP pin input under-voltage protection release voltage VS Temperature

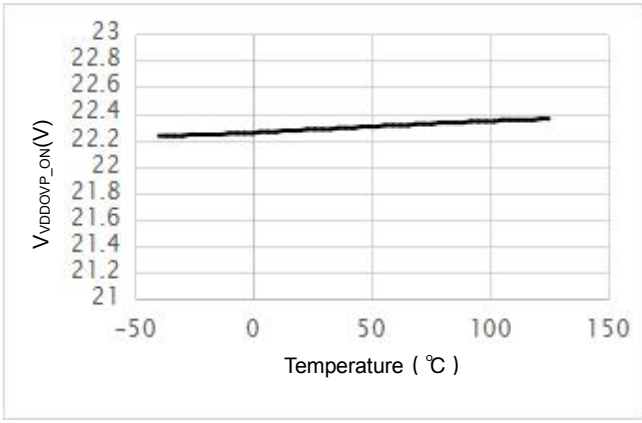


Fig. 11 VDD over-voltage protection voltage（full load）VS Temperature

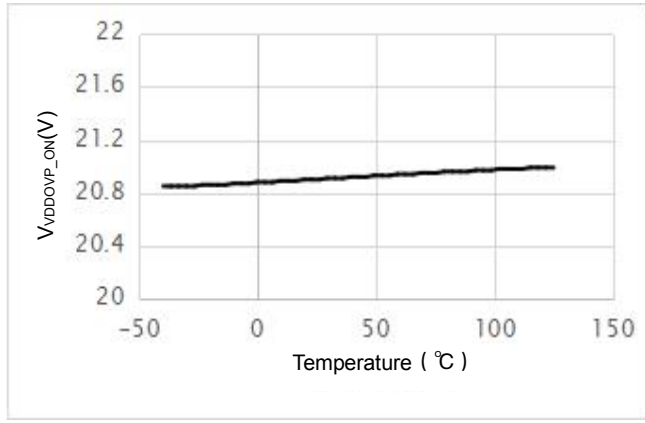


Fig. 12 VDD over-voltage protection voltage (idle load) VS Temperature

Note: unless otherwise specified, typical characteristic curve is obtained under V_{DD}=12V,RI=24kΩ, normal pressure and temperature.

Parameter Measurement Information

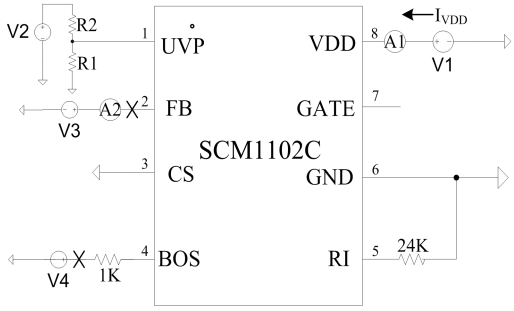


Fig 13 Functional curve test circuit schematic diagram

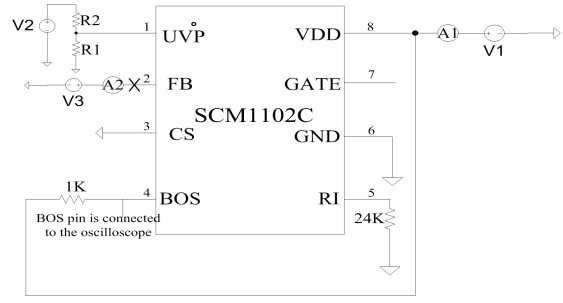
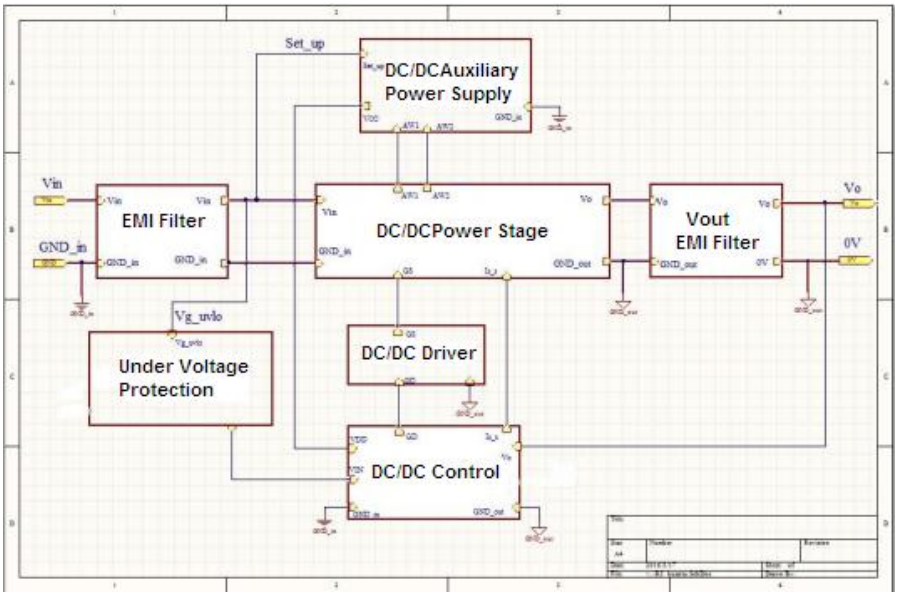


Fig.14 schematic diagram of VDD minimum voltage test required for boost operation

Functional Application



The chip can be applied to flyback topology converters.The functional block diagram is shown on the left.The working principle of this circuit is to store energy to the transformer when the MOS is on,and release energy to the output capacitor when the MOS is off.At the output end,an appropriate Pi filter is used to smooth the square wave pulse into a small ripple dc voltage output,whose value is equal to the average of square wave pulse.

In the output of the circuit,resistance to voltage output voltage sampling,sampling and the sampling error comparator voltage VO to EA place compared with the positive input vlotage comparator benchmark,the error of the amplified voltage VEA through optical coupling is input to the IC FB side,and the other end(in-phase input)of current signal(sawtooth wave signal),thus controlling the duty ratio,and then through the conduction of the totempole output pulse drive MOS and shutoff,realize the stability of the output voltage.

Chip Description

SCM1102C is a highly integrated current mode PWM controller, applicable for DC-DC isolated converter. Its most important features are: first, under light load, it reduce frequency as load reduces, thus it improves light load efficiency.and when it gets close to no load, it works at BURST mode which reduces standby power consumption; second, its protection functions are highly integrated, allowing fewer external devices and reducing PCB area, and ensuring consistency. Third, its minimum operating voltage is 4V.

Unless otherwise specified, numerical value below is typical value tested under normal pressure and temperature, and V_{VDD}=12V,RI=24kΩ.

Oscillator Frequency

Maximum operating frequency of the chip (oscillator frequency) F_{MAX} can be set up by RI pin external resistance, frequency settings satisfy the formula below:

$$F_{MAX}(kHz) = \frac{6890}{RI(k\Omega)} \quad (1)$$

Recommended operating frequency of the chip is between 220kHz and 500kHz (refer to Recommended Operating Conditions for details). If frequency is set up to be too small, RI resistance is big, then RI pin is easy to be interrupted, and minimum frequency will be lower than 22kHz. Under ultralight load, it may create noise; when frequency is set up too high, power consumption of the chip increases, and frequency precision become worse.

When RI pin external resistance connects one capacitance in parallel and earthed, it enables frequency jittering , distributes energy to scope wider than EMI tester bandwidth, and lowers EMI.

Frequency Jittering range is at±6% of maximum set up frequency of RI pin external resistance; frequency jittering period is 6.9ms.

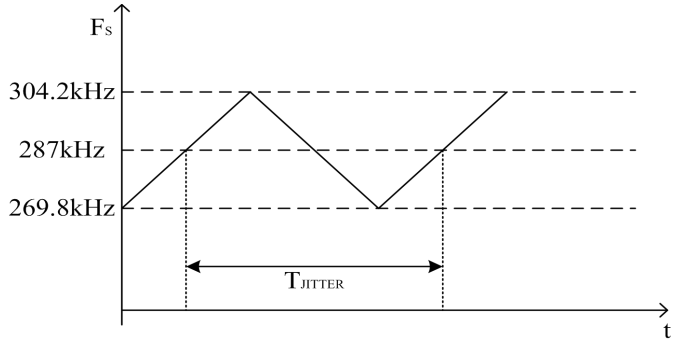


Fig. 15 Diagram of frequency jittering

Built-in Soft Start

The build-in soft start realized by controlling V_{FB} voltage increasing slowly. The issue of overshoot during starting up will be decreased. After soft start, V_{FB} will not be restricted by soft start circuit. The first start and each restart after protection can perform initialization effectively, ensure that both power-on start and restart after protection revocation have soft start.

Intelligent Green Mode

SCM1102C adjusts oscillator frequency by detecting FB port voltage V_{FB}, that is, adjusting frequency of chip output signal GATE. When $2V<V_{FB}<3.7V$, chip works in PWM mode, adjust peak voltage of CS pin only, frequency is the highest and constant; when $1.1V<V_{FB}<2V$, chip enters PWM+PFM mode, which regulates both CS peak voltage and working frequency. As load reduces, frequency lowers gradually; when V_{FB} is lower than 1.1V, chip enters BURST mode, GATE stops output. Curve of work mode changing with V_{FB} is shown in Fig.16.

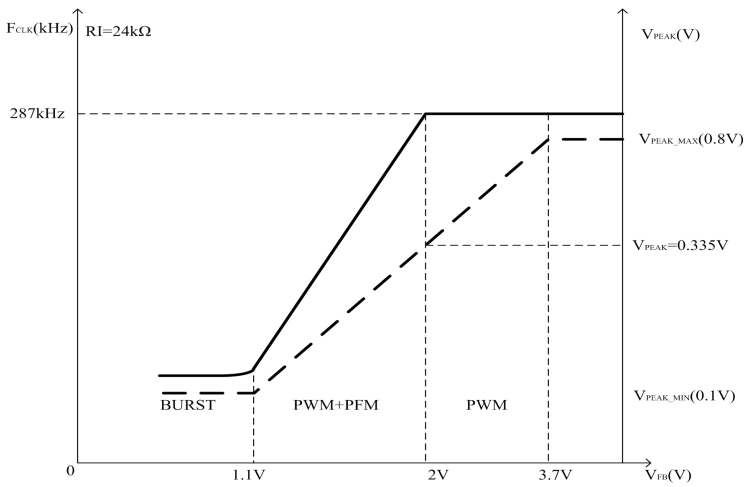


Fig. 16 Intelligent Green mode

BURST Mode

Besides intelligent green ,mode, SCM1102C designed BURST mode internally. When V_{FB} lowers than 1.1V, chip enters to BURST mode, also known as frequency hopping mode. When chip enters BURST mode, chip turns off GATE output. As output load consumption output voltage, opto-coupler current reduces, V_{FB} goes up again. When VFB voltage reaches 1.35V, GATE starts to output pulse. Output voltage of the power supply grow up back to normal after GATE output signal, if V_{FB} is go down lower than 1.1V again, it will enter BURST mode again, and recycling (see Fig.17).

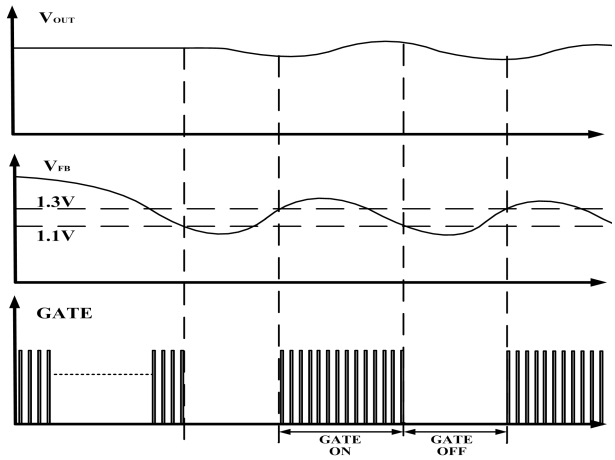


Fig. 17 Related waveform in BURST mode

Feed-forward Compensation

With V_{IN} pin sampling input voltage, generate a compensation voltage V_{RLC} on feed-forward resistance to realize feed-forward compensation and ensure consistency of over current point under high and low voltage.

$$I_{LC} = 5 \times \left(\frac{V_{IN}}{R_{IN1}} - \frac{2.4V}{R_{IN1} \| R_{IN2}} \right) \quad (2)$$

Design of feed-forward resistance R_{LC} can refer to the following formula:

$$R_{LC} = \frac{R_{CS} \cdot T_D \cdot R_{IN1}}{5 \times L_P} \quad (3)$$

Among which

·T_D indicates current detection delay time which includes switch tube turn-off delay.

·L_P indicates primary side inductance of transformer.

·R_{IN1}、R_{IN2} are divider resistance of UVP pin.

·R_{CS} is current sampling resistance.

Built-in Slope Compensation

It adopts two-segment compensation mechanism. When duty ratio is 40%~61%, slope rate is 114mV/μs; when duty ratio is 61%~79%, slope rate is 213mV/μs. This segmented design avoids impact of slope compensation on load capacity. The slope rate above is a typical value measured when RI pin external resistance is 24kΩ.

Input Under Voltage Protection

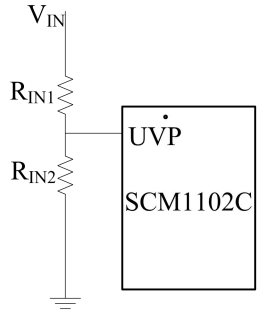


Fig. 18 Electrical block diagram of input under voltage

When $V_{IN} \cdot \frac{R_{IN2}}{R_{IN1}+R_{IN2}} < 1.8V$ enter input under voltage protection;

,

When $V_{IN} \cdot \frac{R_{IN2}}{R_{IN1}+R_{IN2}} > 2V$ revoke input under voltage protection.

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BOS pin Boost Function

If SCM1102C BOS pin connects inductance to input voltage externally and diode to VDD, then it enables BOOST function. BOOST topology is as follows:

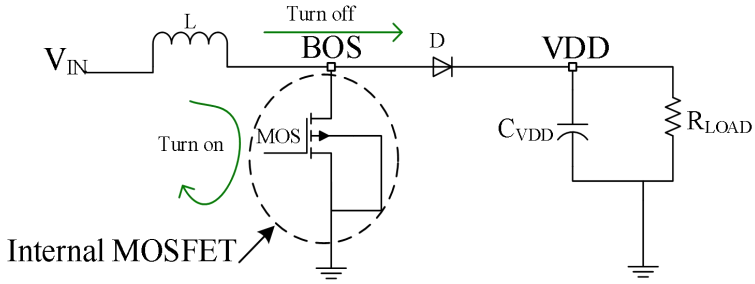


Fig. 19 BOS pin and external inductance and diode constitute Boost topology

1、Inside of BOS module is designed with a high frequency ring oscillator, generates high frequency square signal and controls MOSFET on and off. A constant frequency 1.4MHz and duty cycle 50% were designed Inside of the chip to switch on/off MOSFET. When MOSFET turned on, input voltage, inductance and MOSFET formulate current loop, energy is stored in inductance. When MOSFET turned off, energy stored by inductance is transferred to output port VDD via diode. As before VDD reaching start-up point, current consumption of the chip is low, most current are charging VDD parallel capacity C_{VDD}, making VDD voltage rise up period by period, and startup rapidly.

2、When BOS pin is floating or earthed, BOOST function is not available, the internal start point shall be lower, and VDD needs external starting circuit for power supply.

3、When BOS pin constitutes BOOST connection, if input voltage V_{IN} is lower than VDD under voltage point, then when output voltage is established, add auxiliary winding to supply power to VDD.

4、As VDD voltage rises gradually, BOS module changes from continuous mode CCM to DCM, current for charging VDD shunt capacity reduces gradually, and VDD voltage rises slowly.

5、In event of input under voltage, BOS function is OFF.

6、When VDD reaches start point 15.9V, loop is established normally, BOS function is off; when loop can't be built normally, VDD for BOS function cutoff point is about 17.6V.

7、During normal operation, if VDD falls to V_{UVLO_OFF} point, then BOS function is ON again.

8、If FB pin over voltage protection happens, then VDD falls to 14V, BOS function is enabled again.

FB pin Over-Voltage Protection

When the situation that FB pin voltage V_{FB} being greater than 4.5V lasts longer than T_{D_PL} (refer to electric features, that is $24576T_{OSC}$), then it is considered that FB pin is over voltage. Turn off GATE by force and enter FB pin over voltage protection rest state; if before cumulative time reaching T_{D_PL}, V_{FB} is lower than 4.5V, it will not trigger FB pin over voltage protection; duration of FB pin over voltage sleep state is T_{SLEEP} (refer to electric features, that is $2^{18}T_{OSC}$), after reaching T_{SLEEP}, withdraw FB pin over voltage protection and revoke forced turn off action on GATE, meanwhile soft start reset and pull down V_{FB}. If there is no other protection, chip will soft start again.

Over power protection (OPP)/output short circuit protection (OSP)/open loop protection (OLP) can realize by FB pin over voltage protection, as over power, output short circuit and open loop will cause V_{FB} to rise above 4.5V.

The chart below is a sequence chart of V_{FB} voltage and GATE signal in event of output short circuit. T1 period is soft start process. V_{FB} follows soft start voltage V_{soft} inside the chip; T2 period is FB pin over voltage protection delay time, GATE is not cut off by force; T3 is V_{FB} over voltage protection sleep time; when T3 ends, it enters soft start reset process, and soft start again. When chip starts or restarts, only after passing four rounds internal clock

periods counting, will GATE output pulse. T4 indicates these four internal clock periods, also called initial shield. If output short circuit remains, the above process will repeat periodically.

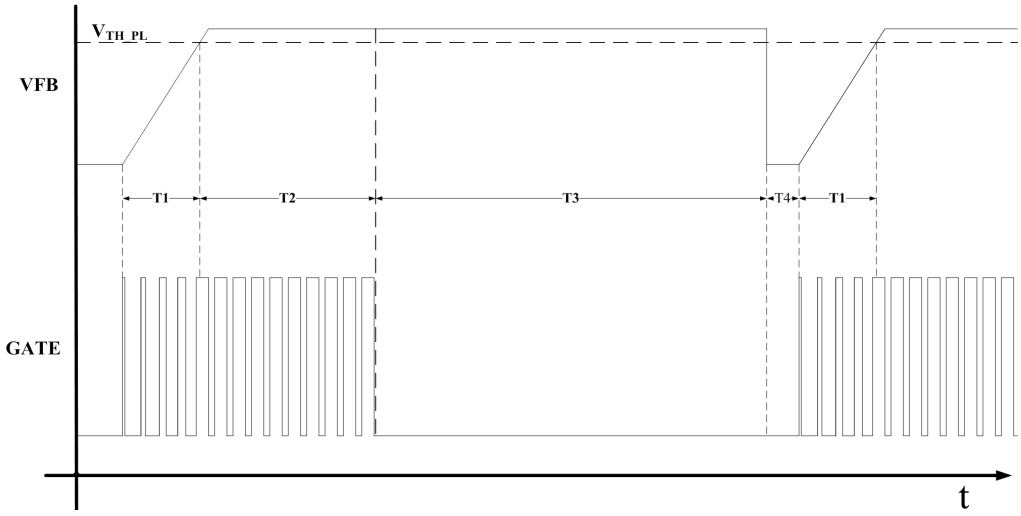


Fig. 20 Sequence chart of V_{FB} and GATE under output short circuit

VDD pin Over-Voltage Protection

If voltage at VDD pin exceeds 22V (over-voltage protection point changes with load, 20V minimum under light load, 23.6V maximum at full load), and lasts for 100μs, then chip enters VDD over-voltage protection state, GATE has no signal output; only when VDD voltage is lower than 15.6V, chip will withdraw VDD over-voltage protection signal, soft start reset. After resetting, proceed soft start process, and GATE outputs normally.

Application Circuit

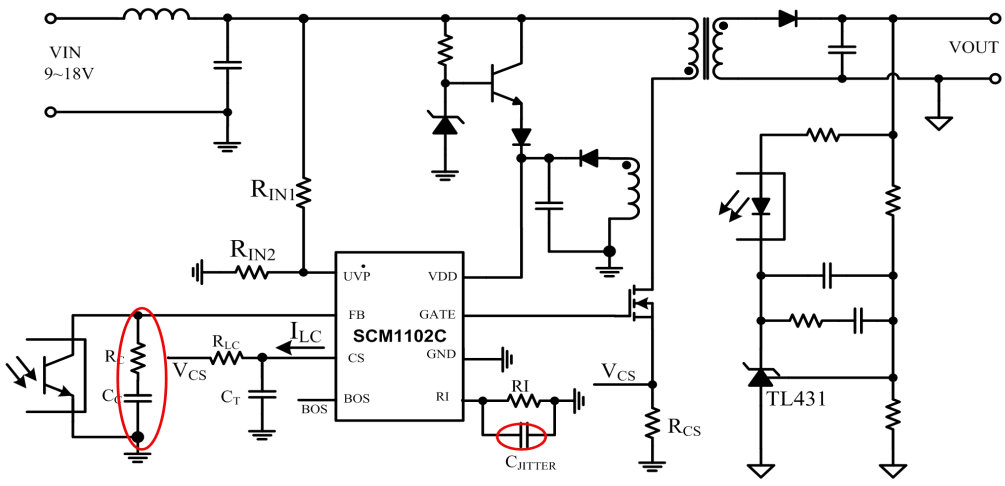


Fig. 21 Typical application circuit 1, BOS pin floats to enable 9V~18V input. Components in the red circle are optional.

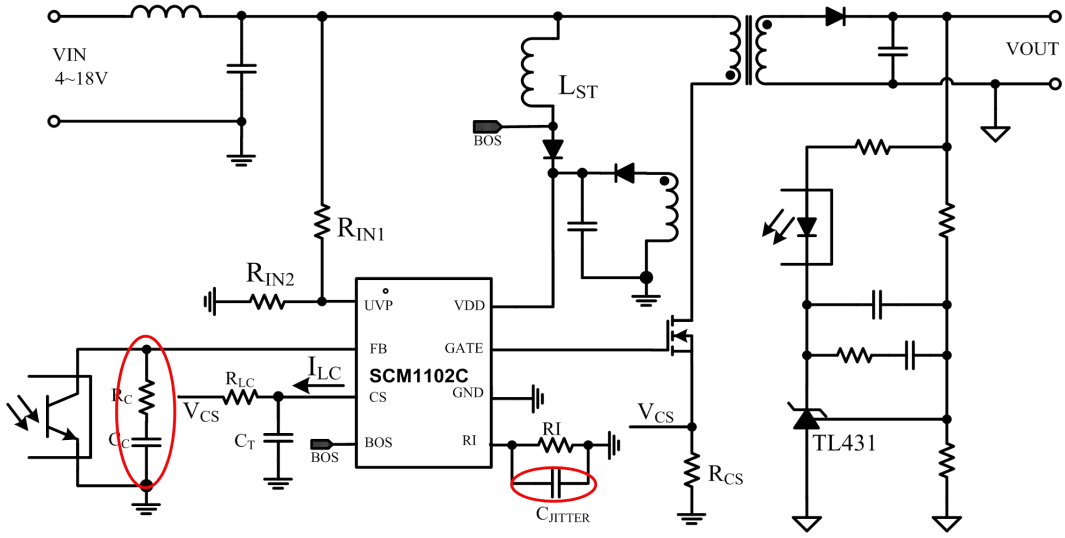


Fig. 22 Typical application circuit 2, BOS pin connects inductance to input and diode to VDD to formulate boost topology and enable low voltage 4V input.

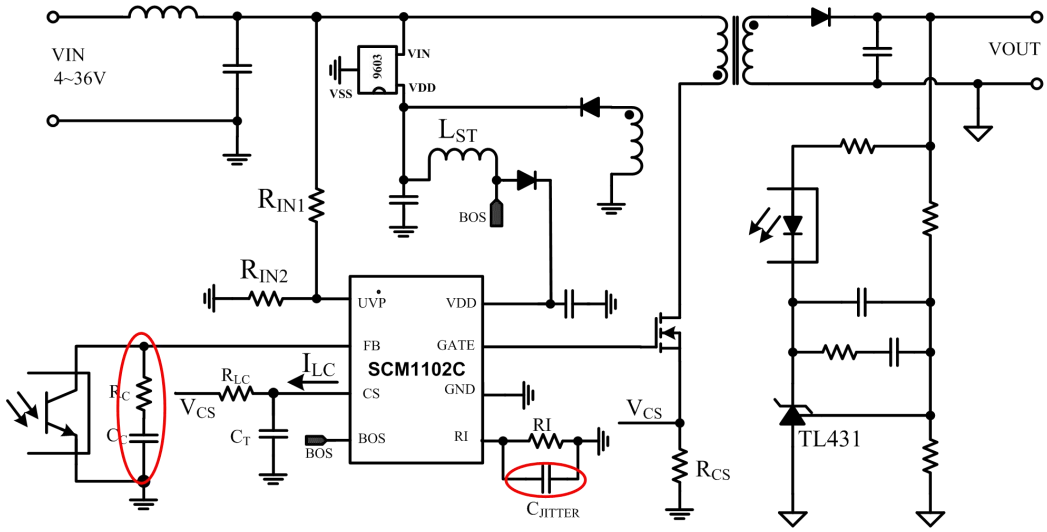


Fig. 23 Typical application circuit 3, externally connected DCDC start-up chip 9603 (SOT-23 Package) to enable whole range input from low to high voltage. Components in the red circle are optional.

Power Supply Recommendations

1.When low voltage input is applied(below 9V),VDD pin bypass capacitor is recommended to be more than 10μF to ensure normal power supply of VDD.

2.BOS pin should be wired as short and straight as possible,away from sensitive signals.

Ordering Information

Part number	Package	Number of pins	Product Marking	Tape & Reel	Weight (1PCS)	Weight (1 REEL include box)
SCM1102CMA	MSOP-8	8	1102C YM	4K/REEL	0.028g	837.2g

Product marking and date code

SCM1102XYZ：

(1) SCM1102,Product designation.

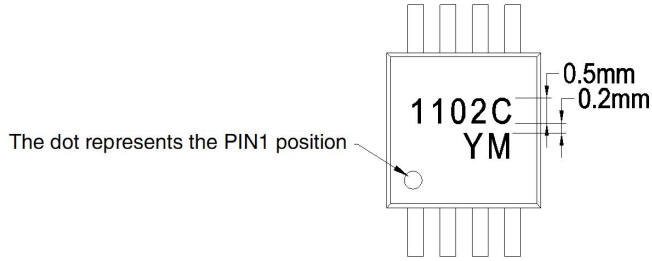
(2) X = A-Z,Version code information.

(3) Y = S,M,Packaging definition code;；S：SOP package；M：MSOP package.

(4) Z = C,I,A,M,temperature level code；C：0℃–70℃,I：–40℃–85℃,A：–40℃–125℃,M：–55℃–125℃.

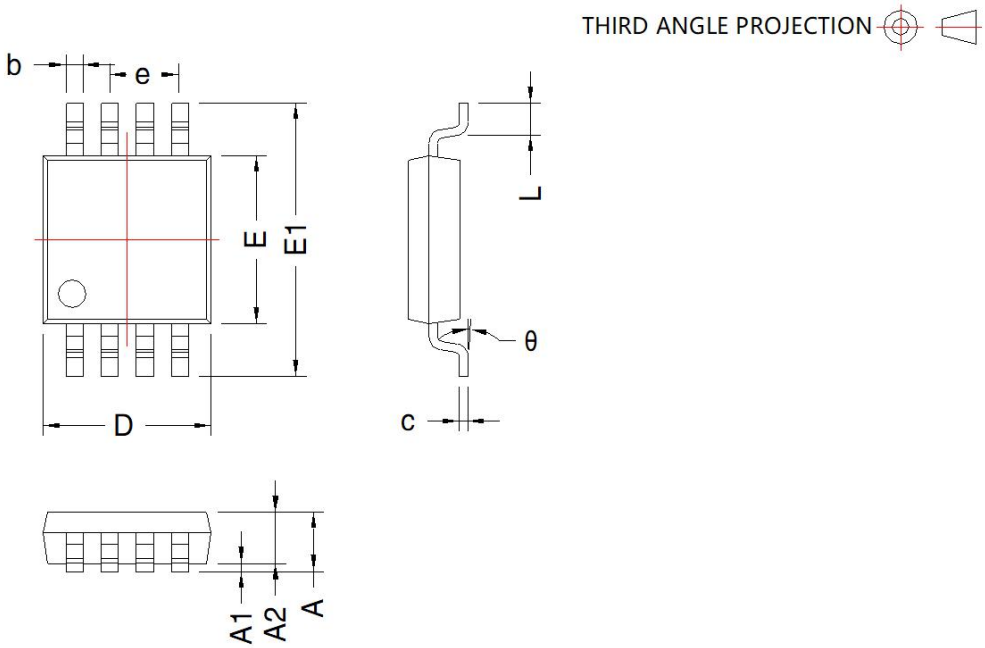
(5) YM：product traceability code；Y indicates product production year code,M indicates product production month code.

Silk Screen Information

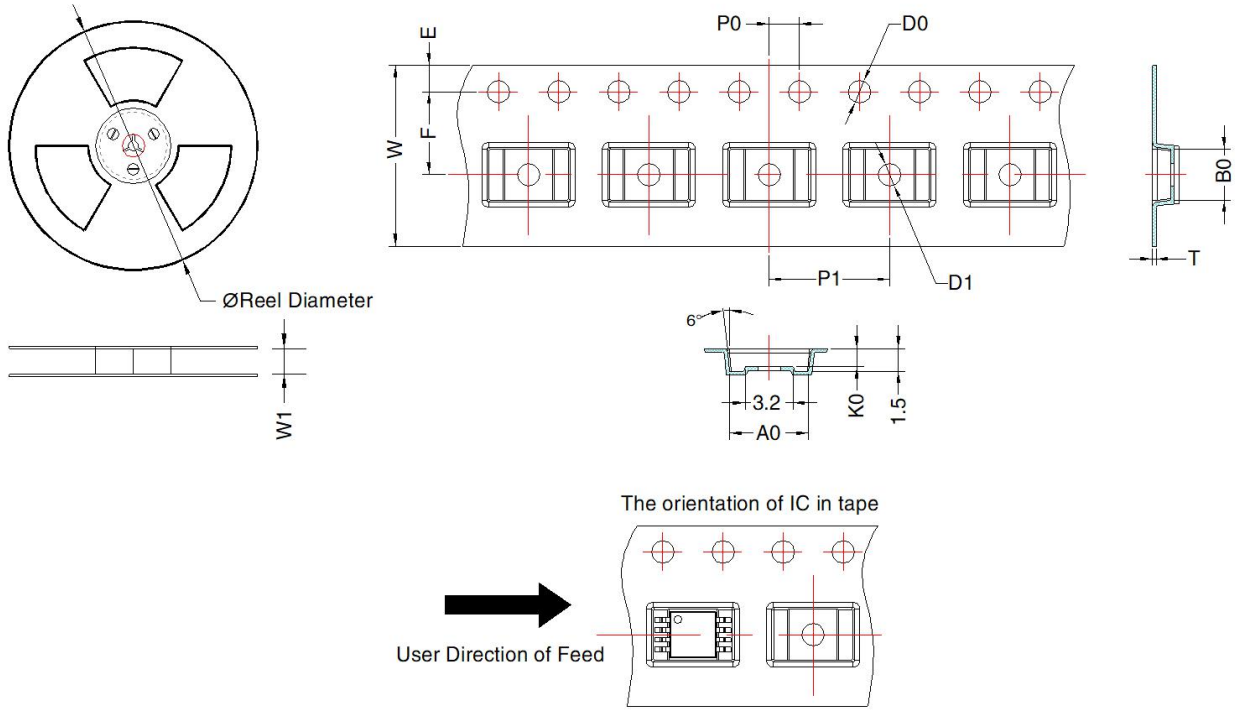


Note:
1、Typeface: Arial;
2、Character size:
Height: 0.5mm, Spacing: 0.1mm, LineSpacing: 0.2mm;

Package Information (MSOP-8)



MSOP-8				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	0.82	1.10	0.032	0.043
A1	0.02	0.15	0.001	0.006
A2	0.75	0.95	0.03	0.037
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
E1	4.75	5.05	0.187	0.199
L	0.40	0.80	0.016	0.031
b	0.25	0.38	0.010	0.015
e	0.65TYP		0.026TYP	
c	0.09	0.23	0.004	0.009
θ	0°	6°	0°	6°



Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)
SCM1102CMA	MSOP-8	4000	330.0	12.4	5.2 ± 0.1	3.3 ± 0.1	1.2 ± 0.1	0.25 ± 0.05	12.0 ± 0.3	1.75 ± 0.1	5.5 ± 0.1	8 ± 0.1	4 ± 0.1	1.5 ± 0.1	1.5 ± 0.1

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